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DESIGN AND ASSESSMENT OF A GRID CONNECTED INDUSTRIAL FULL-SIC CONVERTER FOR 690 V GRIDS

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Design and Assessment of a Grid Connected Industrial Full-SiC Converter for 690 V Grids

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Abstract

Wide bandgap (WBG) power semiconductors have drawn steadily increasing interest in power electronics in the last three decades. These devices have shown the potential of replacing silicon as the default semiconductor solution for several applications in determined power and frequency ranges. Among them, the most mature WBG semiconductor material is silicon carbide (SiC), which presents several characteristics at the crystal level that translate in the potential of presenting lower resistivity, be able to switch faster with lower switching loss, and present both higher characteristics to tolerate and dissipate heat when compared with silicon. However, the same characteristics that make it great also present a different set of drawbacks to be considered, which aligned with its increased cost make it challenging to assess if its advantages are justified for a particular application. Applications that highly value efficiency and/or power density are the most benefited, and converter solutions featuring the technology have already breached into these application markets. However in other applications, the line from which silicon carbide starts making sense in the cost/benefits/drawbacks balance is not clear. This is typically the case of industrial applications, which were the main focus and motivation of this work.

Hence, in this work the main goal has been to determine the basic characteristics, advantages and limitations that SiC technology designs for industrial low voltage high power grid connected converters present. To that end, a 690 V, 240 kVA SiC-based grid-tied converter demonstrator following industrial design criteria has been developed. Then, based on this design procedure a theoretical comparison between a 690 V, 190 kVA SiC-based converter against a silicon-based converter designed for the same power output has been performed to compare them regarding cost, efficiency, size and weight. This work also comprises a thorough revision of the state of art of SiC devices, which led to the selection of the switching device. Additionally, a characterization of both single and parallel-connected operation of the semiconductor modules was performed, to determine the module characteristics and its suitability to build the SiC converter demonstrator.

Results show that the converter demonstrator operates as designed, proving that is possible with the corresponding precautions to achieve: a low inductive power loop, balanced parallel connection of SiC modules, adequate driving circuits for the parallel-connected modules and an adequate filtering solution in compliance with grid-codes based on standard core materials for the selected switching frequency. Finally, the theoretical comparison between the two designed power converters shows that, attained to the conditions of the comparison, the SiC converter solution presents efficiency gains over the whole operating range, while presenting substantial weight savings at 89% of the costs of the Si-IGBT design, presenting itself as the cost-effective solution for the presented application requirements under the given design constraints.

Kurzfassung

Die Bedeutung von Leistungshalbleitern mit großem Bandabstand (Wide Band Gap, WBG) nahm in den letzten drei Jahrzehnten kontinuierlich zu. Diese Bauelemente haben das Potenzial, Silizium (Si) - Bauelemente in bestimmten Anwendungen sowie Leistungs- und Frequenzbereichen zu ersetzen. Siliziumkarbid (SiC)-Leistungshalbleiter sind die gegenwärtig am Weitesten entwickelten WBG-Leistungshalbleiter. Dank besonderer Materialeigenschaften zeichnen sich SiC-Leistungshalbleiter im Vergleich zu Si-Bauelementen durch einen geringeren spezifischen Widerstand, eine höhere Schaltgeschwindigkeit, geringere Schaltverluste sowie eine höhere maximale Sperrschichttemperatur aus. Die deutlich erhöhten Herstellungskosten limitieren den Einsatz von SiC-Leistungshalbleitern auf Anwendungen, in denen die Vorteile dieser Bauelemente die höheren Kosten überkompensieren und Systemvorteile ermöglichen. Heute werden SiC-Leistungshalbleiter z.B. in Solarwechselrichtern oder in Elektrofahrzeugen verwendet. Für Stromrichter industrieller elektrischer Antriebe ist die Kosten-Nutzen-Bilanz des Einsatzes von SiC-Leistungshalbleitern gegenwärtig nicht bekannt. Diese Fragestellung motiviert diese Arbeit. Die Auslegung sowie die daraus resultierenden Vor- und Nachteile eines Stromrichters mit SiC-Leis-tungshalbleitern für elektrische Industrieantriebe ist der Untersuchungsgegenstand dieser Arbeit.

Zu diesem Zweck wurde unter Einhaltung industrieller Auslegungskriterien ein 240 kVA SiC-basierter Stromrichterdemonstrator als aktiver Gleichrichter am dreiphasigen 690 V Niederspannungsnetz untersucht. Auf der Basis einer Stromrichterauslegung für SiC- und Si-Leistungshalbleiter wurde ein theoretischer Vergleich von Kosten, Effizienz, Größe und Gewicht durchgeführt. Die Arbeit stellt zunächst den Stand der Technik für SiC-Leistungshalbleiter dar. Anschließend wird ein geeignetes SiC-MOSFET Module für den industriellen Stromrichter ausgewählt und bezüglich des Schaltverhaltens sowie der Parallelschaltung charakterisiert. Der Auslegung des Stromrichterleistungsteils liegen industrielle Anforderungen zu Grunde. Ein realisierter Demonstrator für einen netzseitigen Stromrichter (Active Front End) ist durch eine symmetrische Parallelschaltung von zwei SiC-Modulen, geeignete Ansteuerschaltungen (Gate Drive Units), eine niedrige Streuinduktivität im Kommutierungskreis sowie ein LCL-Filter mit Standard-Kernmaterialien gekennzeichnet.

Der Stromrichtervergleich zeigt, dass der betrachtete Stromrichter mit SiC-Leistungshalbleitern im gesamten Betriebsbereich geringere Verluste verursacht als ein vergleichbarer Stromrichter mit Si-Leistungshalbleitern. Der SiC-basierte Stromichter ermöglicht auch eine deutliche Gewichtsreduktion bei ca. 89% der Systemkosten. Somit stellen SiC-Leistungshalbleiter eine attraktive technische Lösung für die untersuchte Anwendung eines aktiven Gleichrichters für industrielle elektrische Antriebe dar.

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Nomenclature

ε

- ε_0 : Vacuum permittivity
- ε_r : Relative permittivity

Φ

- Φ_M : Metal work function
- Φ_S : Semiconductor work function
- Φ_{BN} : Schottky barrier height

μ

- μ_n : Electron mobility
- μ_p : Hole mobility

χ

- χ_S : Semiconductor electron affinity

C

- C_T : Tunneling coefficient
- C_J : Junction capacitance
- C_{DC} : DC-Link capacitance
- C_{DS} : Drain-source parasitic capacitance
- C_{GS} : Gate-source parasitic capacitance
- C_{GD} : Gate-drain parasitic capacitance
- C_{iss} : Input capacitance
- C_{oss} : Output capacitance
- C_{rss} : Reverse transfer capacitance
- C_F : Filter capacitors
- $C_{on,sp}$: Specific on-capacitance

E

- E_c : Critical electric breakdown field
- E_g : Bandgap energy
- E_s : Semiconductor electric field
- E_{OX} : Oxide electric field
- E_{on} : Turn-on energy
- E_{off} : Turn-off energy
- E_{RR} : Reverse Recovery energy

F

- f_{sw} : Switching frequency
- f_{res} : Resonant frequency

I

- I_F : Diode forward current
- I_D : Drain current
- I_G : Gatedriver current
- I_{RR} : Reverse recovery current
- I_L : Inductor current
- I_{PWM} : Ripple current

J

- J_s : Saturation current density.
- J_F : Forward current density.

K

- k : Bolzmann constant
- KS: Kelvin source

L

- L : Load inductor
- L_{SR}: Converter-side inductors of the LCL-Filter
- L_N: Grid-side inductors of the LCL-Filter
- L_σ: Stray inductance

N

- N_D : Donor doping concentration
- N_A : Acceptor doping concentration
- n : Electron concentration

P

- p : Hole density
- P_{cond} : Conduction loss
- P_{sw} : Electron concentration
- P_M: MOSFET losses
- P_D: Diode losses

Q

- q : Electron charge

R

- $R_{x,sp}$: Specific resistance of x
- $R_{DS(on)}$: MOSFET turn-on resistance
- R_{th} : Thermal resistance
- $R_{on,sp}$: Specific on-resistance

T

- T_J: Junction temperature
- T_{case}: Case temperature
- T_{amb}: Ambient temperature
- t_{ri} : Current risetime
- t_{fv} : Voltage falltime
- t_{fi} : Current falltime
- t_{rv} : Voltage risetime
- t_{don} : Turn-on delay time
- t_{doff} : Turn-off delay time
- t_{on} : Turn-on time
- t_{off} : Turn-off time

V

- V_n : Saturated electron drift velocity
- v_n : Electron drift velocity
- V_B : Breakdown voltage
- V_{bi} : Built-in voltage
- V_F: Forward voltage
- V_G : Gate voltage
- V_S : Gate voltage in $\alpha\beta$ coordinates
- V_{OV}: Overvoltage
- V_{TH}: Threshold voltage
- V_{DS}: Drain-source voltage
- V_{GS}: Gate-source voltage
- V_{GD}: Gate-drain voltage
- V_F: Diode forward voltage

W

- W_D : Drift layer thickness

Z

- Z_{TH} : Thermal impedance
- Z_{SC} : Short circuit impedance

Acronyms

B

- BHFFOM : Baliga's high frequency figure of merit
- BJT : Bipolar junction transistor
- BOM : Bill of materials

D

- DPT : Double pulse test
- DUT : Device under test

E

- EMC : Electromagnetic compatibility
- EMI : Electromagnetic interference
- ESL : Equivalent series inductance
- ESR : Equivalent series resistance
- ESS : Energy storage systems
- EV : Electric vehicles

F

- FFT : Fast fourier transform

G

- GaN : Galium nitride
- Gnd : Ground
- GTO : Gate turn-off thyristor
- GU : Gate unit, Gatedriver unit

H

- HVDCs :High voltage direct current power transmission systems

I

- IGBT : Isolated gate bipolar transistor
- IGCT : Integrated gate turn-off thyristor

J

- JBS : Junction barrier diode
- JFET : Junction gate field-effect transistor

K

- KS: Kelvin source
- MPS: Merged pin schottky

M

- MLC: Multilayer ceramic
- MOSFET: Metal oxide semiconductor field effect transistor
- MPPF: Metallized polypropylene film
- MPS: Merged pin schottky

N

- NPT: Non punch through
- NTC: Negative thermal coefficient

P

- PCC: Point of common coupling
- PEEC: Partial element equivalent circuit
- PLL: Phase locked loop
- PT: Punch through
- PV: Photovoltaics

S

- SBD : Schottky barrier diode
- Si : Silicon
- SiC : Silicon carbide
- SoC : System on chip
- SPWM : Carrier based sinusoidal pulse width modulation
- SVM : Space vector modulation

U

- UPS : Uninterruptible power supply

V

- VOC: Voltage oriented control
- VSI: Voltage source inverter

W

- WBG: Wide bandgap

1 Introduction

Silicon-based semiconductor switches have shaped the electronics landscape since the very beginning of the solid state revolution. Considered among the most important developments of the 20th century, these devices have been for decades keystone of the electronics industry in all its fields ranging from microprocessors all the way up to power converters. Particularly in power electronics, silicon-based semiconductors enabled the development of Thyristors, GTOs, IGCTs and IGBTs. These components gave engineers active control capability over power demanding applications, hybridizing the power landscape that was for many years dominated by passive self-regulating systems.

Jumping forward to the last decade, a wide array of silicon-based solutions could be found in almost any industrial application there is, and have revolutionized modern society through all the chain of raw material production, manufacture and end usage, while shaping how the required energy is processed within these steps. However, as some applications develop, they also toughen requirements over their conforming power blocks. Higher efficiency and improved power density are driving figures of merit in renewable energy applications, electric vehicles, aircraft/aerospace industry, Energy Storage Systems (ESS), and High Voltage DC transmission (HVDC) among others, which have been powerful drivers of semiconductor technology and power converter development.

Nonetheless, silicon-based semiconductors are reaching limits in terms of some parameters highly regarded by particular applications as these devices struggle when operating under high frequency while handling high power, being normally an engineering task to see how to work around this caveat and balance tradeoffs accordingly. Nowadays, the silicon-based device that is most capable of balancing power handling capability and switching frequency in a blocking voltage range of 600 V-6500 V is the IGBT, which is a bipolar device that presents good conduction loss behavior but suffers from significant loss while switching at high frequency because of its inherent tail current and relatively large rise/-fall turn-on and off switching times which translates in increased switching loss, hurting efficiency and requiring elaborated heat dissipation schemes. Silicon devices also cannot block high voltage without severely increasing their conduction loss, as thicker semiconductors are needed to block higher voltages. In order to avoid this, several alternatives arise as serialization of semiconductors and multilevel topologies, which enable their use at the cost of device derating or higher complexity.

To address these limitations, since the beginning of the nineties a new breed of semiconductors has been in constant development: Wide Band Gap semiconductors (WBG). These semiconductors, as the name suggests, have a wider bandgap for electrons to jump from the valence to the conduction band, providing benefits at the crystal level that translate into thinner, more efficient semiconductors. The most promising WBG semiconductors nowadays are Galium Nitride and Silicon Carbide (GaN and SiC) and both have the potential to replace silicon in the long run in certain voltage, frequency and power ranges.

In this work, the focus is placed on silicon carbide. This material promises sev-

eral advantages over silicon from the 600 V blocking voltage region and beyond. In theory, SiC has a higher thermal conductivity and withstands higher temperatures than silicon, presents increased voltage blocking capability at the same die thickness, and presents lower conduction specific on-resistance and switching loss for the same die size. However, the question of how much of these power semiconductor capabilities can be harvested in converter designs, while sometimes partially answered, is still incomplete regarding total benefits and main design constraints in most industrial converters.

Several applications have started using silicon carbide in their designs in the last years [5], and the main characteristics these early adopter applications share is that efficiency and/or power density add significant value to their market proposal, as the extra cost of these semiconductor devices must be less than what it is to be gained for the particular application figures of merit. Hence, the main early adopters have been so far Electromobility (electric vehicles, traction, and converters for aerospace applications), as they highly profit for power density gains and efficiency, specially in electric vehicles as this provides additional range, which is a defining factor for the end consumer. On the other hand there is also the energy related applications such as renewable energy sources, Uninterruptible Power Supplies (UPS) and energy storage systems, which highly profit from efficiency gains. Some of these applications have the advantage that the converter cost is not usually the main cost driving factor of the application (in solar systems, the solar panels dominate the cost of the bill of materials when compared to the power converters, and the same can be established for lithium batteries in energy storage system), hence the extra cost of the converter is easier to justify when its impact to the application is significant.

However, in more mainstream applications it is harder to determine the cost-benefit boundary from which SiC converters would be a profitable solution to the application. This is also not eased by the fact that device manufacturers typically advertise SiC semiconductor material advantages in contrast with Silicon, which are harder to translate into actual design gains [22, 23]. Or in other cases, when a design is provided, it is then difficult to assess if the design complies with the same requirements a Silicon-based design would, or if a direct comparison would be fair.

Therefore, the main goal of this dissertation is to determine the basic characteristics, advantages and limitations that SiC technology designs for low voltage high power grid connected converters present. And to that end, in this work a SiC based industrial converter demonstrator with grid connection following industrial design criteria has been developed, and then its design has been used as basis to perform a theoretical comparison against a silicon-based converter, which was designed for the same power output. The SiC converter demonstrator requirements abide by the following criteria:

- Topology: Three-Phase two level grid-tied inverter.
- Switching frequency: 20 kHz.
- DC-Link voltage: 1080 V.
- Grid Voltage: 690 V_{ll}.
- Nominal Power: 230-300 kVA.
- Approx. Load current range: [192-251] A_{RMS} or [272-355] A_{Peak}. However, the nominal current value must comply with load scenarios and cause

module average Junction temperatures under 125 °C ($T_J \leq 125°C$ at all times).

- The IEC/TS 62578 harmonic standard must be complied with an LCL-filter.
- Field oriented control and active damping must be implemented.

However, being this project limited in time and not an actual commercial converter design, some simplifications were defined:

- Grid voltage 10% variation was not considered for design purposes.
- Short circuit characterization and analysis will not be discussed in this work, as it is part the PhD work of Jan Schmidt, member of the chair of power electronics of the Technische Universitat Dresden.
- Thorough filter design will also not be discussed in this work, as is it also part of another PhD work of Marcus Mueller, member of the chair of power electronics of the Technische Universitat Dresden.
- Common mode output filter was not considered in this work.

To this end, the Dissertation is divided into the following Chapters:

- *Chapter 2* focuses on the state of art of SiC devices, where a summary of material properties and its semiconductor-based characteristics is presented, followed by an explanation of semiconductors structures built with SiC, and ending with a market summary, to the author's best knowledge, of all off-the-shelf devices in production to the date of study: February 2020.
- *Chapter 3* focuses on the experimentally determined characteristics of the selected SiC based module. Here the device selection criteria is discussed, the measurement methodology is described, and the main results of both single and parallel-connected module characterizations are presented.
- *Chapter 4* tackles converter design, where the main considerations for the SiC based inverter demonstrator is presented. From requirements and nominal parameters to mechanical considerations, this section discusses the main design criteria and limiting constraints, and presents experimental results and data validating the proposed converter demonstrator.
- *Chapter 5* performs a comparison between a silicon carbide and a silicon-based converter. These converters were designed based on the presented methodology, the gathered experimental characterization data and manufacturers data, to present the main advantages and limitations Silicon Carbide based converters inherit from their conforming power blocks and how these fare against the Silicon-based design.
- *Chapter 6* summarizes the main conclusions of the work.

2 Silicon Carbide: Characteristics, Devices and State of Art

In this chapter, an overview of the main characteristics of silicon carbide based semiconductor devices is introduced. First of all, the Silicon Carbide material and its main electrical properties with focus on their impact as building blocks in semiconductor devices is presented. Then, an overview of Silicon Carbide based semiconductors for low voltage, high power applications is performed. Particularly, SiC-MOSFETs and SiC Diodes are presented, focusing on their structure, forward and reverse characteristics, transient characteristics and main working principles. Then, a thorough market study of the evolution of SiC-based devices in the last five years is presented. Here, both discrete and module packaged devices are reviewed with focus on nominal current, voltage ranges, topologies and device developing companies. Finally, a summary of the main applications harvesting the advantages of this technology is presented. Here, the main characteristics that make SiC attractive for each application are introduced and shortly discussed.

2.1 Silicon Carbide

Silicon Carbide is a IV-IV[1] wide band-gap indirect semiconductor material made from carbon and silicon atoms joined through covalent bonds in a 1:1 ratio [1]. These atoms organize themselves with a tetrahedral configuration, and the molecules they form can be layer-arranged in a variety of organized crystal structures called polytypes. There are over 200 different polytypes of SiC crystals [24] and not all of them are used for semiconductor purposes due to the fact that each polytype presents its own unique electrical, optical, thermal, and mechanical properties [25]. Among other uses of silicon carbide, it is used as an industrial abrasive for non-ferrous materials, and to produce very hard ceramics [26] due to its inherent diamond-like hardness (Mohs 9/10). Over the last three decades, the most studied polytypes for semiconductor applications were the polytypes named 4H, 6H and 3C. Today the 4H polytype is the most widely used crystal configuration for semiconductor purposes as it presents a wider bandgap, good isometric electrical properties and a higher Baliga Figure Of Merit (BFOM) when compared to other polytypes, indicating its potential for lower conduction loss and hence better suitability for semiconductor applications. Both an example of the material and the most studied crystal arrangements for power electronic purposes can be found in Fig. 2.1.

As a matter of fact, only 4H and 6H polytypes have ever seen industrial manufacturing, as the production process in order to control the polytype is quite challenging when considering other structures. Hence in this work, it can be assumed that when a reference to SiC is made, it is referred to its 4H polytype.

[1] Two elements belonging to the group IV of the periodic table

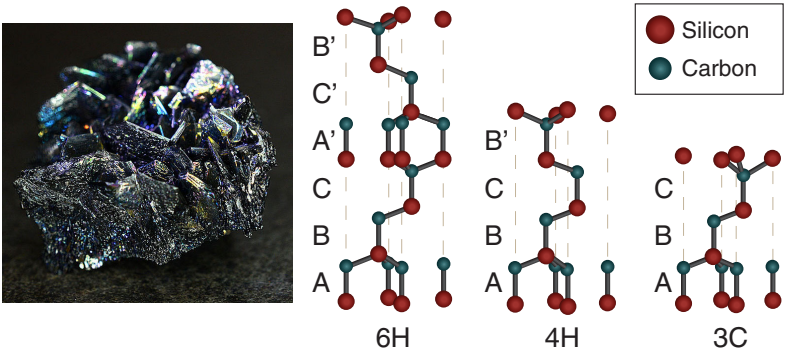

Figure 2.1: Left: Silicon carbide crystal. Right: Most studied silicon carbide polytypes for power electronic purposes. Based on [1].

2.2 Overview Characteristics of SiC compared to Si

As portrayed by several figures of merit for semiconductor materials [27], Silicon Carbide presents outstanding electrical properties [28–31] which have been summarized in Fig .2.2.

These material characteristics infuse SiC-based semiconductors with several advantages when compared with their silicon counterparts, and among these the 3 main benefits are:

- Higher efficiency at higher blocking voltages.
- Higher temperature operation capability.
- Higher switching frequency capability.

However, these device characteristics are rooted on material electrical properties, which is why these characteristics are to be discussed and clarified in the following sections, in order to get a grasp on their origins.

- Effects of higher critical electric field E_C

  The critical electric field of silicon carbide is approx. 10 times higher than on silicon, which makes SiC an excellent choice for power semiconductor devices. According to (2.1), which describes the breakdown voltage in an ideal unipolar semiconductor [9], it is dependent on the critical electric field E_C and the thickness of the depletion layer (also referred as depletion width) W_D.

$$V_B = \frac{W_D E_C}{2} \tag{2.1}$$

  From (2.1), and using the data in Fig. 2.2, it can be concluded that the de-

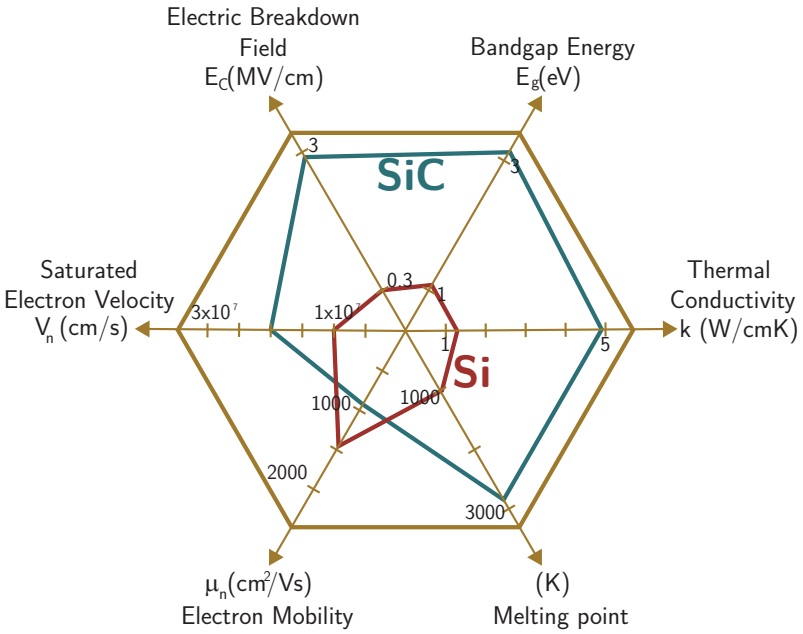

Figure 2.2: Comparison of silicon carbide (4H polytype) and silicon main characteristics.

pletion width can be 10 times thinner than a traditional silicon device. Additionally, according to (2.2) [9], which describes the doping of the drift region under breakdown voltage condition, the doping can be increased 100 times when compared to silicon.

$$N_D = \frac{\varepsilon_0 \varepsilon_r E_C}{qW_D} \tag{2.2}$$

The fact that in SiC the semiconductor results on a thinner device with a higher doping level impacts the specific on-resistance $R_{on,sp}$, which in ideal conditions is defined by (2.3) [9]. This equation finally determines that even though electron mobility in Silicon is higher, SiC specific on-resistance is almost 3 orders of magnitude smaller than silicon. All as a result of its higher critical electric field.

$$R_{on,sp-ideal} = \frac{W_D}{q\mu_n N_D} \tag{2.3}$$

Replacing 2.1 and 2.2 in 2.3, the expression can be rewritten in function of the breakdown voltage as seen in (2.4). This famous expression allows to use

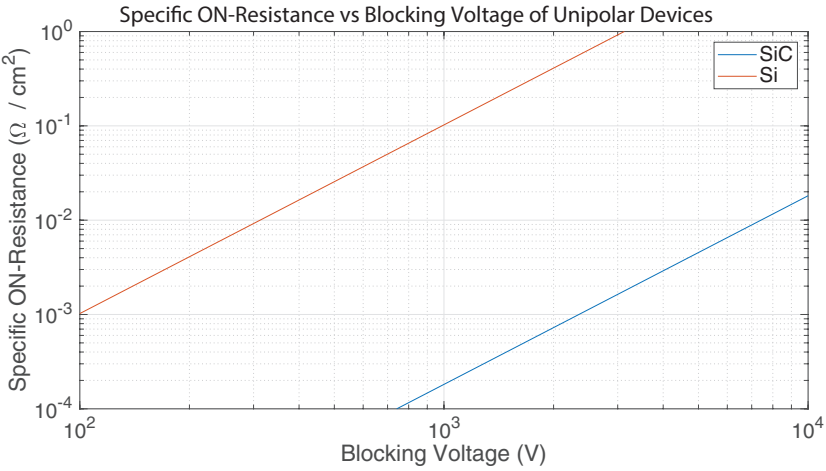

Figure 2.3: Specific on-resistance of SiC and Si unipolar devices vs blocking voltage in an ideal N-type drift layer.

the data from Fig. 2.2, particularly critical electric field and electron mobility, to estimate the specific on-resistance of semiconductors vs breakdown voltage, as seen in Fig. 2.3.

$$R_{on,sp-ideal} = \frac{4V_B^2}{\varepsilon_0 \varepsilon_r \mu_n E_c^3} \tag{2.4}$$

In summary, the main advantages of SiC higher critical electric field in ideal unipolar semiconductors are:

- Higher blocking voltages for the same specific on-resistance, or lower specific on-resistance for the same blocking voltages.
- Thinner devices than in silicon.
- Higher doping concentration capability.

- Effect of temperature characteristics in devices

  Silicon carbide presents a thermal conductivity of over 3 times higher than silicon. Furthermore, at room temperature it is higher that of any metal. Additionally, this material presents higher melting temperature, and lower intrinsic carrier concentration due to its bandgap [9], as it can be observed in Fig. 2.4. This means that these devices can run hot without risking destruction of the device by having a comparable concentration of intrinsic carriers with ionized dopant concentrations. In that case, the device is no longer controlled by the dopant-introduced carriers, but from its intrinsic carriers, which generate a positive feedback loop (more carriers → more heat → more carriers) that generates a thermal runaway. This effect is much less likely to happen in silicon carbide devices, being its junction operating temperature mostly limited by packaging technology. In Fig. 2.4, it is possible to observe that

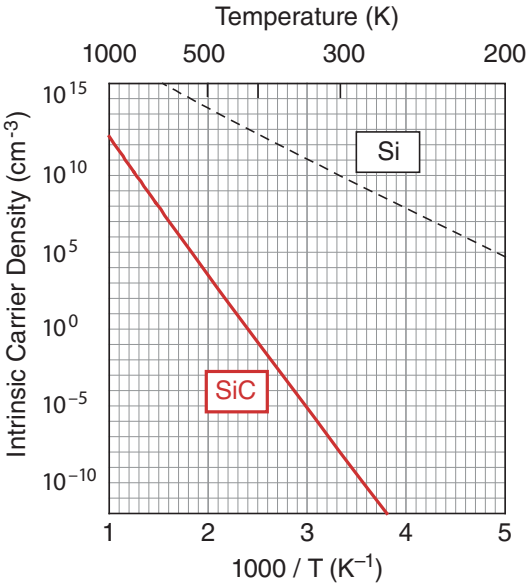

Figure 2.4: Arrhenius plot of the intrinsic carrier density of SiC and Si. ©2015 The Japan Society of Applied Physics. Source: [2, 8].

close to 500 K (220°C) the intrinsic carrier concentration of silicon can be close to $10^{14}/cm^3$, which could rival with lightly doped semiconductors, and therefore destroy the devices. On the other hand, silicon carbide must operate close to 500°C to present the same intrinsic carrier concentration that silicon presents at room temperature.

- Higher operating frequency capability of SiC based devices

  SiC devices are more suited than silicon devices for operating at high frequency while handling power. This potential was foreseen by Baliga's figure of merit for high frequency operation devices BHFFOM [27] (see (2.5)). This figure of merit aims to minimize overall loss, considering $R_{DS(on)}$ based conduction losses and switching losses as a function of the input capacitance C_{iss}, which needs to be charged/discharged to change the switching state of the device. This higher operating frequency capability is also implied in its high saturation electron velocity [32].

$$\text{BHFFOM} = \frac{1}{(R_{on,sp})(C_{on,sp})} = \frac{1}{\left(\frac{4V_B^2}{\varepsilon_0 \varepsilon_r \mu_n E_c^3}\right)\left(\varepsilon_0 \varepsilon_r \frac{E_c}{2\sqrt{V_G V_B}}\right)} = \mu_n E_c^2 \frac{\sqrt{V_g}}{2V_B^{1.5}} \quad (2.5)$$

- Improved material ruggedness effects

  SiC is not only lightweight, but it is also chemically inert and corrosion-

resistant. It is not attacked by any acids, molten salts, or alkalies even when exposed to temperatures up to 800°C [26]. SiC presents a very low coefficient of thermal expansion and is very stiff [32], featuring a 9-9.5/10 hardness index on the Mohs scale. These features, along with its high temperature operation capability makes SiC attractive for a range of rugged applications, including military systems and electronics for oil wells, geothermal plants, and robotic spacecraft [33].

- Higher Current Density

  The current density of unipolar SiC devices is two to three times the maximum current density of unipolar silicon devices [34] as a result of higher thermal conductivity and lower loss, due to lower specific on-resistance.

- Higher Reliability of SiC Devices to Cosmic Radiation

  The big bandgap of silicon carbide makes it more difficult to generate electron-hole pairs by ionizing radiation, as an electron in the valence band requires three times the energy that was required in silicon to jump the energy gap. Particularly, SiC-MOSFETs react better to neutrons or heavy ions than Si-IGBTs [35]. In [35] the author presumes that the wider bandgap acts as a shield to radiation that otherwise could affect the behavior of the semiconductor, improving reliability against single event burnouts. To that end, SiC-MOSFETs were tested under ionizing radiation values equivalent to 4000m above sea level with no damaged parts, providing FIT values that were at least four orders of magnitude better than comparable Si-IGBTs.

2.3 SiC-Based Semiconductor Devices

The timeline of SiC-based devices started at the beginning of the XXI century with the world's first SiC Schottky Diode, and since then these devices have evolved rapidly, as it can be seen in Fig. 2.5. With the exception of the SiC-PiN diode and the SiC-BJT, (which also exist as off-the-shelf devices in small numbers) unipolar devices such as SiC-based SBDs, MOSFETs and JFETs have dominated development and market share, and are the ones considered when referring to comparisons between SiC and silicon. In Fig. 2.6. a diagram of the main competition areas of the most prominent semiconductor material technologies for power electronic applications is presented.

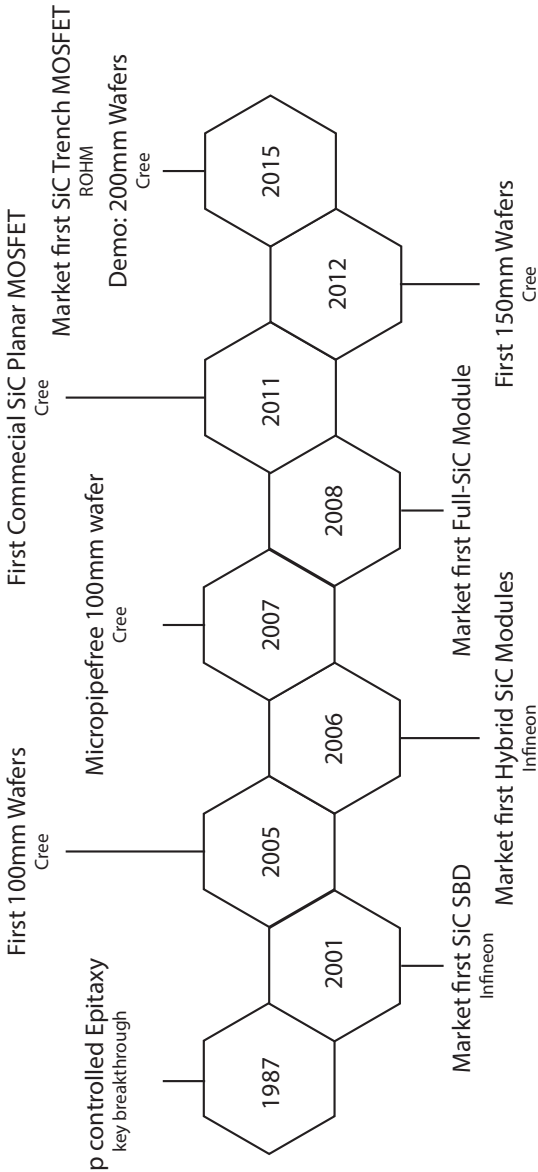

Figure 2.5: SiC semiconductor timeline. Based on [3–6].

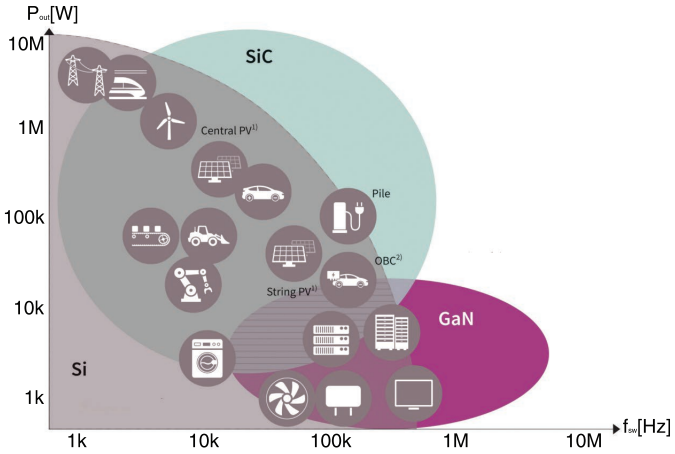

Figure 2.6: SiC, Si and GAN power/frequency competition space. Source: Infineon [7].

Nonetheless, other devices have been studied as well. SiC-IGBTs [36–38] have been studied, mainly to characterize its behavior and prove its functionality, but their potential remains to be seen, as it is difficult to assess and foresee if they will be able to compete with unipolar SiC based design solutions [39]. SiC-Thyristors have also been seen in research [40, 41] showing promising results and improvements in efficiency when compared with their silicon counterparts, but they have not been seen in manufacturer roadmaps or off-the-shelf devices so far. The same goes for SiC-GTOs [42], showing improvements over silicon-based designs but not appearing in market horizon so far.

A clear overview of the device voltage ranges can be found in Fig. 2.7. Based on these voltage ranges, and since the focus of this work is on low voltage high power SiC based power converters, only unipolar SiC devices such as the SiC-MOSFET and the SiC Schottky Barrier Diode (SiC-SBD) are going to be further discussed. The major exception here is the SiC-JFET, which will not be discussed because it is a normally-on device, which is not preferred for most power converter designs. This fact has also driven the semiconductor industry away from them, going from being the most popular SiC switch in 2012 to its state nowadays, where only one company actively develops them as an off-the-shelf device. This will be further discussed in the market overview section.

2.3.1 SiC Diodes for Low Voltage Applications

As previously discussed, SiC diodes were the first devices to exist as a commercial solution. Nowadays however, there are three main SiC diode structures in the market, Schottky Barrier Diodes (SBD), Junction Barrier Diodes (JBD) and P-Intrinsic-N Diodes (PIN)[2]. However, this last structure is reserved for medium-

[2]A more accurate name for pin diodes would be Pn-N Diodes, as the middle layer is a lightly doped structure and not an intrinsic one

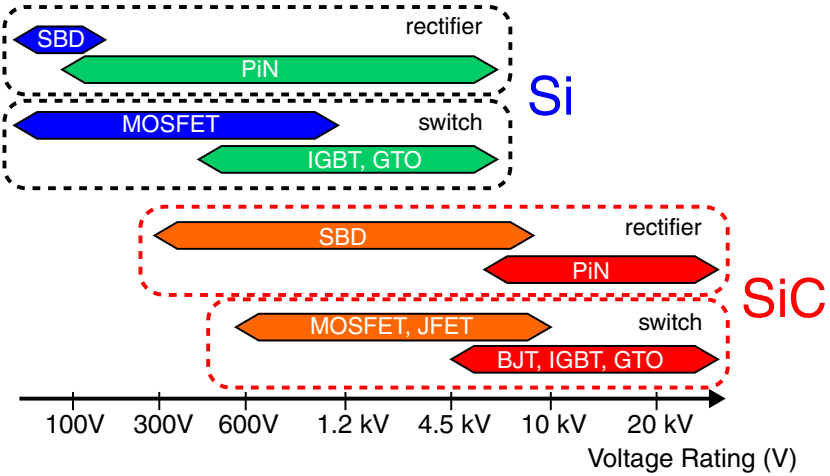

Figure 2.7: Major territories of individual unipolar and bipolar power devices for Si and SiC in terms of the rated blocking voltage. ©2015 The Japan Society of Applied Physics Source: [8].

high voltage applications, and therefore will not be covered in this work. For further reading, the reader can refer to [43].

The SiC Schottky Barrier Diode (SBD)

The traditional Schottky barrier diode is a unipolar device, as it only consists on a metal in contact with a doped semiconductor, typically N-type, and therefore there are no elements that can inject minority carriers (typically holes) to the semiconductor device, hence being a majority carrier device. Since there is no P-type material to form a PN junction, another mechanism must be employed to achieve rectification. The rectification in a normal diode is made through energy band bendings at the junction, which generates a voltage that acts as barrier. In the case of Schottky diodes, this is achieved by using metals with distinctive work function that, when compared to the electron affinity of the semiconductor, bends the band diagram of the semiconductor. This generates a built-in potential V_{bi} that acts as a barrier for electrons to travel from the semiconductor to the metal (or from the other point of view, a current from the metal to the semiconductor) (see Fig. 2.8). Typically, both in silicon and silicon carbide, the electron mobility of electrons is higher that of holes, as the effective mass of holes is higher. This influences the conductivity of the material, which is proportional to the doping concentration, the electron charge and the carrier mobility, explaining why N-type semiconductors are preferred for the drift layer.

The basic structure of the Schottky barrier diode can be found in Fig. 2.9. In it, the metal contacts, the drift region and the substrate can be observed. Since in metals the electric field is always zero, electrons present themselves only on the surface (or in this case, in the metal-semiconductor interface), and therefore the

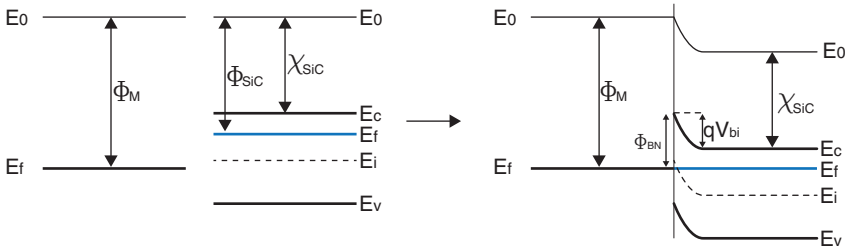

Figure 2.8: Band diagrams of the metal-semiconductor junction. Left: In isolation. Right: Joined in thermal equilibrium. Based on [2, 9, 10].

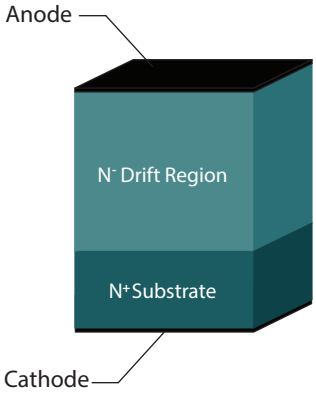

Figure 2.9: Schottky barrier diode internal semiconductor structure.

structures to withstand an electric field during the off-state are the drift region and the substrate. From here, two possible design options are available. Either the drift region depletion layer allocates the electric field, so that the voltage drop falls completely in the drift region (triangular electric field, Non-Punch-Through design NPT), or the thickness and doping of the drift layer are adjusted so the device is thinner and the electric field penetrates the highly doped substrate, (trapezoidal electric field shape, Punch-Through design PT). Most books and analyses to understand the inner workings of the device explain the NPT design as its expressions are less complex when compared with a non-uniform electric field. Nonetheless, most power devices are built as punch through [44], which in SiC is especially understandable as the highly doped substrate is necessary to build the drift layer, which is grown over the substrate in a layer by layer process called epitaxy, which is very expensive. Therefore, since a PT design will lead to lower specific on-resistance, and make a thinner device reducing its already high cost, would make sense to do so.

Due to the fact that the built-in voltage V_{bi} depends on the work function of the metal, it can also be adjusted to obtain better forward characteristics depending

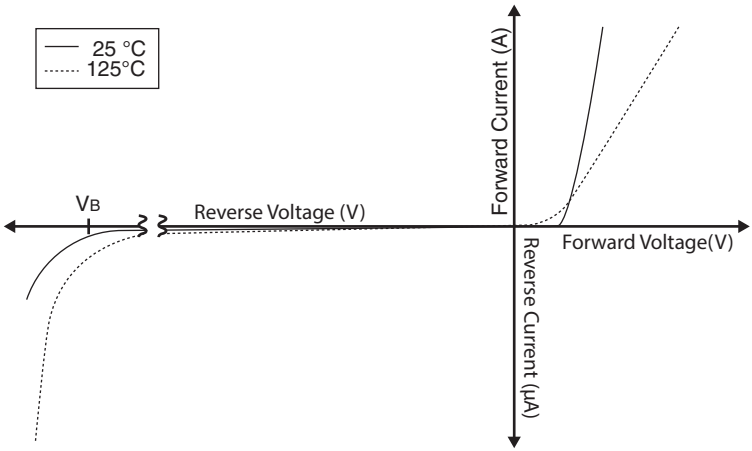

Figure 2.10: Forward and reverse characteristics of the SiC-SBD.

on the metal that is used to generate the junction. For example ideal low-current characteristics of platinum on SiC present a built-in voltage of 0.85 V and titanium on SiC a 1.27 V. In contrast a normal SiC P^+N junction presents a 2.7 V built in voltage [10], which is one of the reasons why SiC Schottky diodes are preferred if the blocking voltage allows its use. The static characteristics of Schottky diodes can be found qualitatively in Fig. 2.10. And afterwards, its quantitative behavior is discussed.

- Forward Characteristics:

  Forward characteristics of SiC Schottky diodes are governed by (2.6) [10] which is the same expression for a traditional PN junction. However, in contrast with the PN junction, in the case of the Schottky junction, the saturation current J_s is defined by the expression (2.7) [10]. Therefore, the variables dominating the current density in function of voltage are the Schottky barrier Φ_{BN}, which by looking at Fig. 2.10 equals to $\Phi_{BM} = \Phi_M - \chi_S$, and the Richardson constant A. The Richardson constant was studied specifically related to SiC with Schottky diodes in [21], and it is from this study that the values from [10] were based. This constant varies according to the metal with which the junction was made, and its values associated with some of these metals can be found in Table 2.1[3].

$$J(V) = J_s \left(e^{\frac{q(V - V_{bi})}{kT}} - 1 \right) \tag{2.6}$$

$$J_s = AT^2 e^{\frac{-q\Phi_{BN}}{kT}} \tag{2.7}$$

[3]Reverse characteristics of the table have been ignored, as most books only refer to the forward values, possibly because the reverse characteristics of the diode are not dominated by thermionic current flow, but electron tunneling and Schottky barrier lowering

Table 2.1: Richardson's constants for several metal contacts for SiC N-type semiconductors [21].

Metal	φ(eV)	A(A/cm^{2}K^2)
Ta	1.03	300
Ti	1.27	400
Ni	1.4	150

However, both in [9] and [8], a modified Richardson constant is used, which is calculated as $A^* = 4\pi q m^* \frac{k^2}{h^3}$ in which m^* is the Carrier effective mass, k is Boltzmann's constant, and h is Plank's constant. Using this expression in 4H-SiC renders a constant $A^* = 145 A/cm^2K^2$, which would be close to the Nickel contact of Table 2.1. Nonetheless, trying to find the original references, [9] is ultimately based on [45], and in it the origin of this value is not further clarified. On the other hand, [8] citation chain leads to the original work presented in [46], which does not mention values for the Richardson constant. Therefore, the method proposed in [21] would be recommended to assign a value to the Richardson constant as it is more up to date regarding the original work of the other sources and it is based in experimental results.

Finally, (2.6) relates the current with the voltage drop on the metal-semiconductor junction, however, this junction is only comprised of the lightly doped N-drift layer and the metal. Additionally, to get the total forward voltage it must be considered that this N-drift region is built over a thick n+ substrate (which is required for handling, and to make a quality ohmic contact with the metal cathode [47]) and metal contacts. In other words, the ohmic drop of substrate, the contacts and the drift layer must also be considered.

Hence, the final expression of the forward voltage is:.

$$V_F = \frac{kT}{q} \ln\left(\frac{J_F}{J_s} + 1\right) + R_\Omega J_F \tag{2.8}$$

in which $R_\Omega = (R_{drift,sp} + R_{substrate,sp} + R_{contact,sp})$.

It is interesting to remark, that since the junction voltage increases with the logarithm of the current density (see (2.8)), and the ohmic part increases linearly with current density, for high forward currents the logarithmic part is small when compared with the ohmic and the voltage starts increasing linearly, following the ohmic part. This explains why in SiC-SBDs, the forward characteristics look more linear than classic silicon diodes. It is not because of the material, but because most SiC diodes are Schottky diodes operated with high current densities.

- Reverse Biased Characteristics:

  The reverse characteristics of the Schottky diode also obey (2.6), but experimental results show that the expression alone deviates in several orders of magnitude regarding leakage current [9]. This is due to two effects, Schottky barrier lowering and electron tunneling [10]. Schottky barrier lowering is an effect that is produced under high electric fields and an energy barrier. The concept behind it is that the electron on the semiconductor should diffuse to the metal, as the energy is lower there, but the electric field counteracts

it. This can be understood as a positive "mirror image" charge on the metal that attracts the electron. This effect lowers the Schottky barrier slightly, increasing the leakage current [9]. Additionally, due to high electric fields close to the breakdown voltage, impact ionization (effect responsible for avalanche multiplication beyond the breakdown voltage) produces additional electrons that can tunnel through the barrier. Therefore, considering all effects, the final expression is [9]:

$$J_s = AT^2 e^{\frac{-q\Phi_{BN}}{kT}} e^{\frac{q\Delta\Phi_{BN}}{kT}} e^{C_T E_M^2} \tag{2.9}$$

Where $\Delta\Phi_{BN} = \sqrt{\frac{qE_M}{4\pi\varepsilon_0\varepsilon_r}}$ is the decrease in the Schottky barrier,

$E_M = \sqrt{\frac{2qN_D}{\varepsilon_0\varepsilon_r}(V_R + V_{bi})}$ is the maximum magnitude if the electric field in function of the reverse bias voltage V_R, and C_T is a tunneling coefficient. According to [9], in Silicon Carbide a $C_T = 8 \cdot 10^{-13} cm^2/V^2$ generates results consistsent with experimental observations.

The final aspect of the curve is the breakdown voltage V_B. This voltage is defined as the reverse voltage V_R at which the critical electric field E_C is reached, and therefore over this value avalanche breakdown should follow. In practice however, datasheets tend to specify this value at around 80% of the absolute critical electric field of the device [10] due to design safety margins. The avalanche breakdown process is produced by impact ionization, which is an effect that refers to electrons and holes that, subjected to an electric field, gain enough energy to generate electron-hole pairs upon collision with atoms in the lattice. These new electron-hole pairs can cross the depletion layer as a form of leakage current, generating heat in the process, which elevates the energy of the system, hence more electron-hole pairs can be generated leading to an avalanche effect. The derivation of this effect is described in [9], but basically consists on analyzing impact coefficients, which are a definition that describes the number of electron-hole pairs that a carrier traversing the depletion region in 1cm deep can generate. With these impact coefficients an expression to find the total number of electron-hole pairs generated by a single electron-hole pair at a distance x from the junction can be found (known as the Multiplication coefficient), and with it, the condition for this equation to rise to infinity can be found (indeterminate the denominator). Based on that, the critical electric field expression is determined. This critical electric field is doping density dependent, and is expressed for SiC by [9]:

$$E_c = 3.3 \cdot 10^4 N_D^{1/8} \tag{2.10}$$

and with it, (2.1) can then be solved.

- Switching characteristics:

  The main switching effects in diodes come from traditional definitions based on a PN-diode and these effects are called forward recovery and reverse recovery. Forward recovery occurs during the turn-on transient, and it consists in increased voltage drop and hence, additional loss during the turn-on event. Since the flow of minority carriers is finite and not instant, during the turn-on

transient there is not enough of them to produce conductivity modulation[4], and therefore the diode experiments a higher resistance than in steady state, hence generating higher loss on the device during this transient. A similar effect plays a role during turn-off, when the reverse recovery takes place. Since now the junction is flooded with carriers, it is necessary to get rid of the stored charge in order to generate the depletion region to block the voltage. Hence this stored charge generates a current during this transient, which reaches its peak when the device reaches the blocking voltage it needs to block in the circuit. Therefore, this reverse recovery current generates additional losses during the transient, both in the diode and in other potential circuit elements along the path (e.g. SiC-MOSFETs) of this current.

Both of these effects are non-existent in Schottky diodes, as it is a majority carrier device and therefore no minority carriers are required for conductivity modulation effects. Hence there is almost no loss during switching events in theory. The only stored charges in the junction are attributed to the junction capacitance [12]. This junction capacitance arises from the depletion region, which acts as a dielectric for the free charges moving at both sides of the junction (this is the classical definition of a capacitor, free charges separated through a dielectric). The derivation of this junction capacitance comes from the definition of the specific capacitance, which is $C_{sp} = \frac{\varepsilon_0 \varepsilon_r}{d}$, in other words, dielectric constant over distance of the plates, which in this case is the depletion region. The expression for the junction capacitance is:

$$C_J = \frac{\varepsilon_0 \varepsilon_r}{W_D} = \frac{\varepsilon_0 \varepsilon_r}{\sqrt{\frac{2\varepsilon_0 \varepsilon_r}{qN_D}(V_R + V_{bi})}} \tag{2.11}$$

Additionally, from an implementations perspective, Schottky Diodes require a structure to prevent the formation of high electric fields in the edges of the metal. This would degrade the breakdown voltage and increase the leakage current, which is why a typical approach is to build a P-type guard ring to protect the edges [9]. This P-ring generates a parasitic PN junction in parallel with the Schottky diode, but since its on-state voltage is higher than of the Schottky diode, it should remain unbiased as long as the voltage drop in the Schottky diode is lower than the on-state voltage of the parasitic PN junction. Therefore, this effect should be negligible.

In summary, the SiC-SBD is a diode with low forward voltages, and negligible reverse recovery charge. However, it can present significant leakage current, and although it can be controlled to some degree by design of the Schottky barrier and the critical electric field, it can still generate undesired loss during blocking. Therefore, an intermediate solution between a PiN and a Schottky diode has been presented, which is called the SiC Merged Pin Schottky Diode (SiC-MPS).

[4] In PiN junctions, when in on-state, minority carriers injected in the lightly N-type doped region are designed to surpass its doping concentration. In this case the specific resistance of the drift region does not obey ohms law anymore, and instead it is dependent on the mobility of electrons and holes, and the minority carrier lifetime. This change in the specific resistance due to both types of free carriers in the drift region is called conductivity modulation. [9]

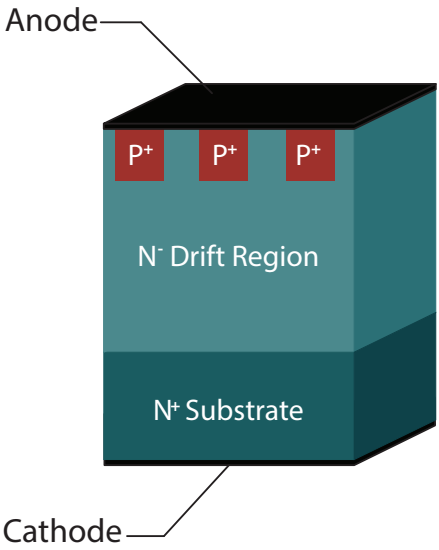

Figure 2.11: MPS Diode internal semiconductor structure.

The SiC Merged Pin Schottky Diode (MPS)

The MPS diode, also known as JBS (Junction Barrier Schottky), is a Schottky diode in which small P-type islands have been included in order to protect the device in reverse blocking operation. It presents lower leakage current and enables forward mode high current surges [10]. A diagram of its structure is presented in Fig. 2.11.

An in-depth discussion will not be performed here as it behaves essentially like a Schottky Diode. Some adjustments to the forward and reverse current characteristics must be considered as the effective area of conduction is smaller (the P+ islands do not conduct in normal operation, and therefore they reduce the current path area when compared to a Schottky device of the same active chip size). Thus, the JBS presents a higher voltage drop than a Schottky diode, but lower than a PiN diode of the same area (for more information please refer to [47]). When considering reverse characteristics, it shows less leakage current as the P+ islands generate a depletion region that prevents the formation of high electric fields on the metal-semiconductor junction. Finally, regarding reverse recovery characteristics, when operated with currents so that the voltage drop does not forward-bias its parallel PN junction it behaves like a Schottky diode, which is the case of most SiC-JBS Diodes on the market. However, if high currents are used so that the resistive component of the forward voltage dominates and forward-biases this PN diode, it can present recovery charge.

Additionally, in [2] a difference between JBS and MPS Diodes is made, remarking that MPS Diodes contain the P+ islands but are designed to never conduct except during turn-on, increasing its surge withstand capability, making the de-

vice behave like a Schottky Diode otherwise. On the other hand, JBS Diodes are made of the same structure but are designed to function in PiN operation in parallel with the Schottky diode. This usually happens on devices of higher blocking voltages (>3kV) in which instead of the junction, the main component of the forward voltage is the n-drift resistance, raising the voltage rapidly to the point of forward-biasing the PN junction of this Diode, being inherent to the design that the JBS diode behaves hybridly.

This can be observed in Fig. 2.12. In 2.12.a, several reverse recovery curves for a 1200 V SiC-MPS diode can be observed being necessary to use 15 times the rated current to generate reverse recovery effects. On the other hand, in Fig. 2.12.b, a comparison of the reverse recovery of a 3.3 kV SiC-SBD, SiC-JBS, and SiC-PiN diode can be observed, in which it is clearly visible that the SiC-JBS presents some recovery charge in normal operation.

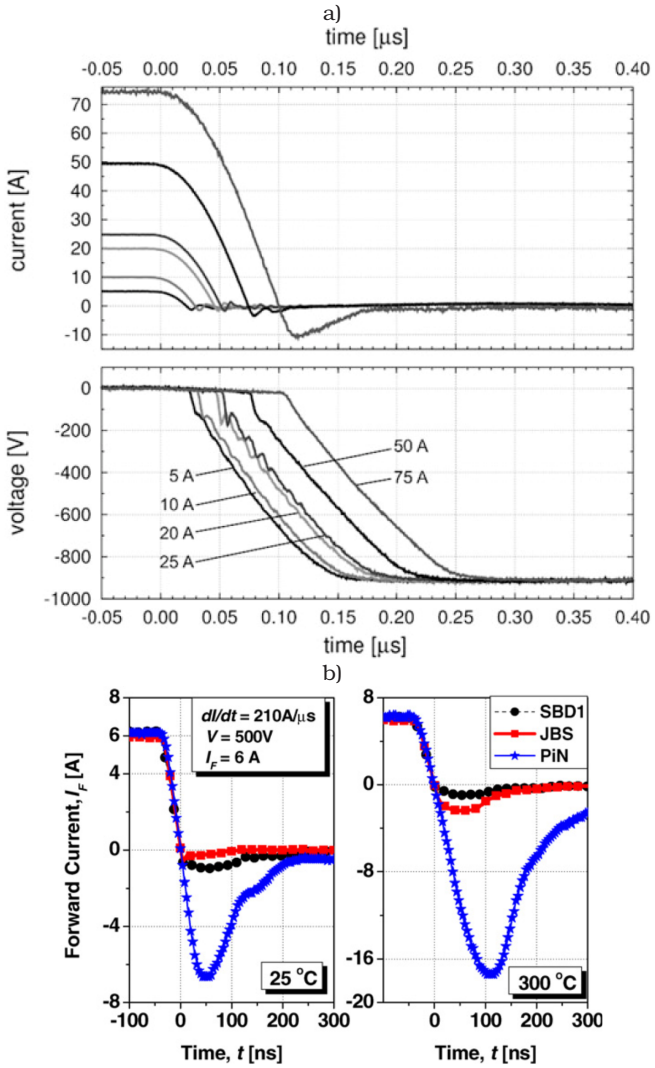

Figure 2.12: Reverse recovery characteristics of different diode structures. a) Reverse recovery characteristics for a 5 A 1200 V rated SiC-MPS Diode. Reprinted from [11] ©2015, with permission from Elsevier. b) Comparison of different reverse recovery characteristics for a 3.3 kV SiC-SBD, JBS, and PiN diodes. ©IOP Publishing. Reproduced with permission. All rights reserved. Source: [12].

Finally, according to [48], the SiC-MPS structure was born more as a result of necessity than improvement. The main problem of the first SiC SBDs was surface defects in crystals, which then presented structural problems when transformed into a semiconductor-metal junction. These structural imperfections were prone to generate uneven electric field distributions, which led to points of increased leakage currents. In other words, it generated hotspots that could lead to the destruction of the device. Therefore the JBS structure was proposed, and with it the Electric field on the metal-semiconductor junction border was reduced, being the critical point now at the lower height of the P+ regions. Nowadays most SiC Schottky devices are MPS in structure [48], with the sole exception of low voltage variants that are designed with the goal of decreasing cost. In [48], it is also mentioned that to distinguish them, as the information is rarely available on the datasheet, a comparison of repetitive surge current and reverse leakage currents can be performed. Devices with SiC-MPS structures should present surge ratings of at least twice the value of normal SiC-SBDs of the same rated current and less leakage current.

But then. What does difference SiC Schottky diodes and Silicon Schottky diodes? The answer is mainly rooted in its $R_{DS(on)}$ resistance. In order to block high voltages in silicon the device had to be too thick, and therefore the $R_{DS(on)}$ was too high. Furthermore, any PN junction included to protect the device would lead to hybrid behavior. This is why silicon Schottky diode blocking voltages are on the 100-300 V range, in contrast with SiC Schottky diodes, which are typically in the 600 to 1700 V range.

2.3.2 SiC-MOSFETs for Low Voltage Applications

As of 2020, there are two main SiC-MOSFET semiconductor structure concepts on the market, the planar MOSFET and the trench MOSFET. Nonetheless, both devices have similar operation mechanics, and therefore the planar SiC-MOSFET will be used as example to be discussed in detail, and afterwards the main characteristics and differences of the trench version will be introduced.

The Planar Vertical MOSFET

The planar vertical MOSFET gets its name due to the fact that the gate is built over the channel and semiconductor crystal. As it can be observed in Fig. 2.13, the gate oxide and the gate are built over the P-type and the n-drift region, using positive voltages to invert the characteristics of the P-type material and attract electrons to the oxide surface, generating the channel. Therefore, the current path goes from drain to source as the following: drain → substrate → drift region → accumulation region[5] → channel → N+ → Source. Hence, and although there are P-type semiconductor areas in this device, as they do not inject holes to conduct electricity the MOSFET behaves as a unipolar device. This means, conductivity modulation effects do not occur and no recombination of minority carriers occurs.

To understand how the channel is built, and hence, how the MOSFET works, it is necessary to tend to the band diagrams, which are presented in Fig. 2.14. In

[5]This is the part of the n-drift region that sits right below the gate, and its carrier concentration also gets affected by the gate voltage, presenting therefore a different resistance than the drift region

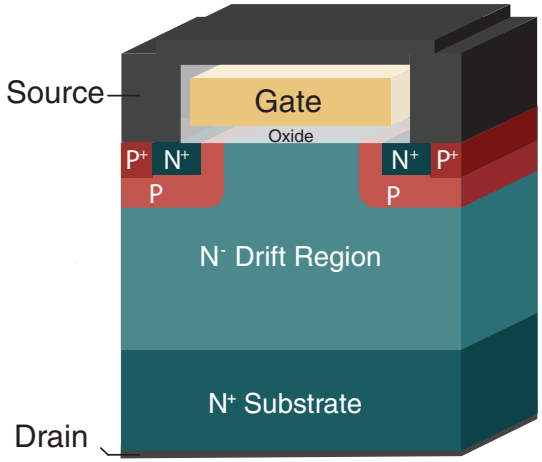

Figure 2.13: Planar vertical MOSFET semiconductor structure.

this example it is assumed that a metal with a Fermi level higher than the Fermi level of the P-type semiconductor has been used to build the device. Thus, the default state of the MOSFET is depleted without external voltage ($V_{TH} > 0$). In other words called enhancement mode MOSFET, which is a normally-off device. The alternative is called depletion mode MOSFET $V_{TH} < 0$, but they are not widely used in power electronics, as normally turn-off devices are preferred for safety reasons. In this example it can be seen that if a negative voltage is applied the Fermi level of the metal rises, which generates an electric field that unbends the energy bands in the semiconductor, hence more holes are attracted to the oxide surface, state that is called accumulation mode. If, on the other hand, the voltage is increased, at certain point the intrinsic Fermi level bends under the Fermi level of the semiconductor. This means that now direct next to the oxide the semiconductor presents a Fermi level that is over the intrisic Fermi level of the material, hence behaving as N-type. This process is called inversion, and the threshold voltage V_{TH} is then defined as the voltage that needs to be applied to the gate in order to make $\varphi_{FN} = \varphi_{FP}$ (or in other words, $2\varphi_{FN} = \varphi_s$). This is known as strong inversion [9], and from there it can be assumed that the amount of mobile charges next to the oxide are enough to be used to form the channel.

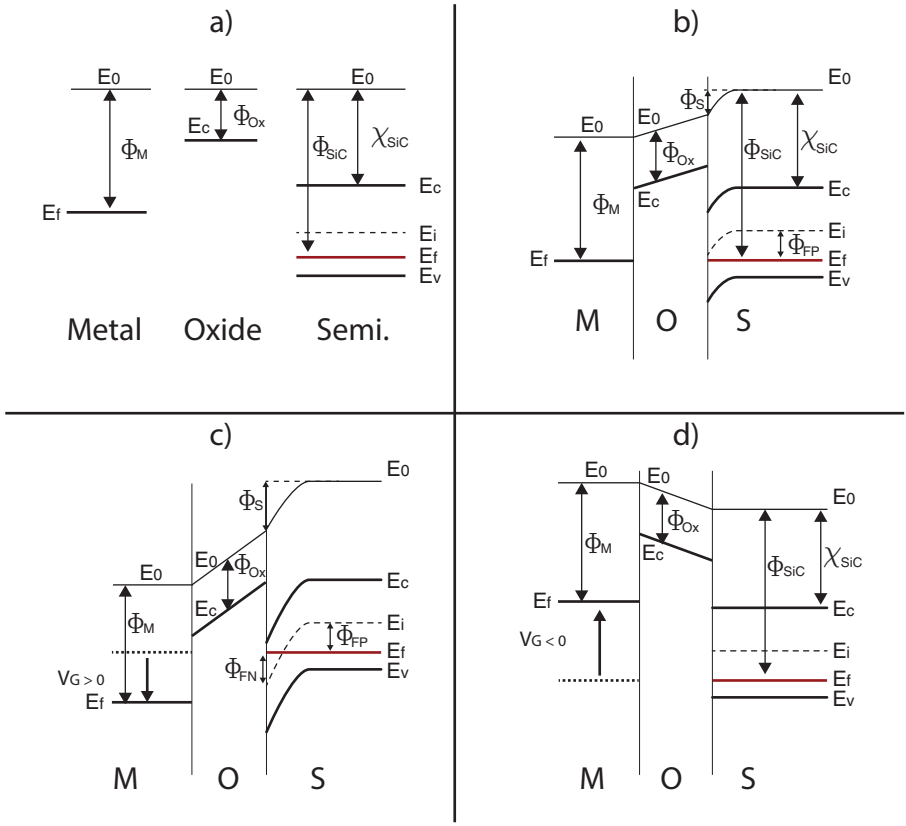

Figure 2.14: Band diagrams of the MOS capacitor. a) Metal, oxide and semiconductor levels in isolation. b) MOS capacitor in thermal equilibrium (enhancement mode). c) MOS capacitor under positive voltage bias (inversion mode), note that if $\varphi_{FP} = \varphi_{FN}$ then the applied voltage is the threshold voltage. d) MOS capacitor under negative voltage bias (accumulation mode), note that a slight bending due to extra holes can happen if the negative voltage is increased. Based on [9].

Nowadays, instead of metal a polysilicon structure is used, as it can withstand higher temperatures required by the wafer manufacturing process and its work function can be tweaked through doping [9], which allows to control the threshold voltage. In order to make an enhancement N-type MOSFET, an N-type polysilicon gate electrode and a P-type semiconductor are preferred to form the channel.

The threshold voltage can then be derived from the band diagrams as the voltage drop on the oxide, which is modeled as a capacitor, plus the voltage required to produce the band bending necessary to generate the strong inversion. This calculation is made in [47] and it is calculated as follows:

$$V_{TH} = \frac{\sqrt{4\varepsilon_0\varepsilon_r kTN_A \ln(N_A/n_i)}}{C_{ox}} + \frac{2kT}{q}\ln(N_A/n_i) \tag{2.12}$$

If discussing the MOS capacitor[6], then it is necessary to discuss the gate oxide, which is crucial in order to make the MOSFET work. Typically, the oxide material used is silicon oxide SiO_2, as silicon is already present in both silicon and silicon carbide, so it is relatively straight-forward to build it over the semiconductor. This oxide has an energy bandgap of 9 eV, and a critical electric field of 10 MV/cm. However, for reliable use without degradation, fields no higher than 4 MV/cm should be applied [2]. In the same source, and based on Gauss law, the ratio of electric fields obey the ratio of dielectric constants as:

$$E_{OX} = \frac{\varepsilon_S}{\varepsilon_{OX}} E_S(x = 0) \tag{2.13}$$

Since $\frac{\varepsilon_S}{\varepsilon_{OX}} \approx 2.5$ (for both SiC and Si), the electric field in the oxide can be 2.5 times the electric field in the semiconductor. This was not an important issue in silicon, as the critical electric field is close to 0.3 MV/cm. However, as SiC devices present higher electric fields, the limit of reliable use of the critical electric field of SiO_2 can be easily reached. This raises additional concerns about the reliability of the gate oxide in SiC devices, especially when considering that the gate oxide on first generations of SiC devices was made even thinner to improve channel mobility, which was very poor due to traps generated in the semiconductor-oxide interface. Furthermore, the tunneling current through the oxide at high electric fields contributes to dielectric breakdown, and it is higher on SiC than Si because the offset between bands is smaller in silicon carbide MOS capacitors. Nowadays, several technologies and careful screening processes have enabled reliable use of the gate to some extent [35], and it is possible to get SiC-MOSFETs to the same low ppm rate as Si-MOSFETS or Si-IGBTs [10]. However more thorough studies to assess the question of gate oxide reliability and longevity properly require extensive data, and no such study has been conducted so far [2].

This is one of the main reasons why the first batch of SiC-MOSFETs were planar devices. Trench devices are a well known, proven technology in silicon devices, presenting lower on-resistance and requiring less material. but in SiC they were not a straightforward implementation as the gate oxide observes a high electric field at the corners of the trench. Hence, planar devices were introduced, as

[6]The MOS capacitor is the gate-oxide-semiconductor structure that allows the inversion of the semiconductor material

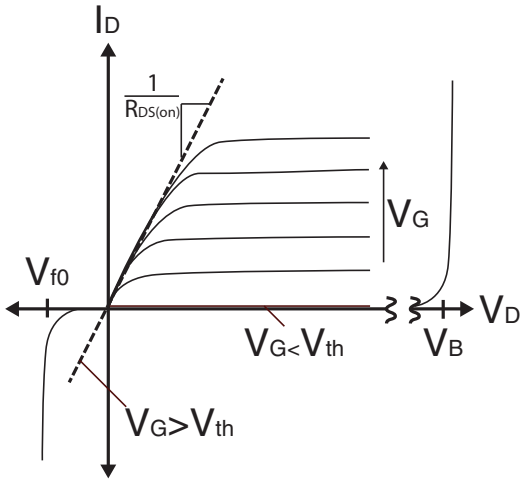

Figure 2.15: Forward and reverse characteristics of the SiC-MOSFET (enhancement mode).

planar devices present inherently a P-type semiconductor to build the channel, which also shields the gate oxide from high electric fields inherently.

Finally, a qualitative figure for the forward and reverse characteristics of the MOSFET can be found in Fig. 2.15. If the gate voltage is kept below the threshold voltage of the device, the device does not conduct in the first quadrant, conducting only in the third quadrant as a forward-biased diode, which is made through the PN junction that is formed between source and drain, hence called body diode. However, as explained in [10], the inherent band bending of the channel already helps to turn this diode on, which is why its knee voltage is smaller than the expected $\approx 2.7\,V$ that a SiC PN junction should typically present. Negative gate voltages are necessary to unbend the bands (Fig. 2.14.d) and see the real knee voltage of the diode.

Now, if the gate voltage is higher than the threshold voltage, then the MOSFET starts conducting. However as long as the drain-source voltage is over $V_{GS} - V_{TH}$, the electric field generated by V_{DS} will interrupt the channel; the current saturates for a defined gate-source voltage and the MOSFET operates in pinch-off state. On the other hand, if V_{GS} reaches its recommended turn-on value, the channel will present its rated $R_{DS(on)}$. Therefore the voltage drop on the device should be much smaller than $V_{GS} - V_{TH}$, and hence the device will conduct in the first quadrant in the linear operation area (ohmic behavior).

- Static Characteristics

  The derivation of the I/V characteristic of the MOSFET is defined by (2.14). and it is based on assuming a charge traveling through the channel in a lateral device. Its derivation is presented in most books but in summary, it consists in considering that the charges that form the channel, do so in the

form of a capacitor, and they will move at the speed of the majority carriers of the material $v_n = \mu_n E$. With these two ideas it can be easily derived.

$$\begin{aligned} I_{DS} &= \frac{Q}{\Delta T} \\ &= \frac{C(V_{G-CH} - V_{TH})}{L/v_n} \\ &= \frac{A\varepsilon_0\varepsilon_r}{t_{ox}} \frac{(V_{G-CH} - V_{TH})}{L} \mu_n E \\ &= \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right) \end{aligned} \tag{2.14}$$

However, in [10], a more complete expression, originally published in [49], describes a more thorough characteristic considering additional effects such as the depletion region that forms below the channel. This expression can be found in (2.15). In it, the depletion capacitance C_D is also used and it is expressed in (2.16).

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left((V_{gs} - V_{TH}) V_{DS} - \frac{1}{2} \left(1 + \frac{C_D}{C_{ox}} \right) V_{DS}^2 \right) \tag{2.15}$$

$$C_D = \sqrt{\frac{\varepsilon_0 \varepsilon_r q N_A}{2\Delta V_{TH}}} \tag{2.16}$$

However, in ohmic region, this equation is not a good approximation, as it models the channel in function of the voltages V_{DS} and V_{GS}, hence being accurate as long as most of the voltage drop befalls on the channel. However as the device enters the ohmic region, the contributions of all resistances mentioned in the current path must be considered.

In reverse mode, the MOSFET functions in three ways. If the channel is off ($V_{GS} < V_{TH}$), then the MOSFET behaves as a PN diode (body diode) as described by (2.6), but with the saturation current expression that is derived for traditional PN-junctions (please refer to [10] for further information). If however the channel is in on-state, then the resistive behavior of the channel is present, and here two possible operation modes arise. If the voltage drop in the channel is smaller than the PN-junction built-in voltage, then the channel conducts alone. On the other hand, if the voltage drop is higher than the forward-bias voltage of the diode, then both current paths will share the current. This action of turning on the device in third quadrant is also known as synchronized rectification.

Additionally, some modules feature a SiC Schottky diode in parallel to the MOSFET. The reason for this is threefold. First, the Schottky diode will present a lower knee-voltage than the body diode, presenting lower loss and allowing current distribution between devices in third quadrant. Second, the Schottky diode is a unipolar device, and therefore will not present the reverse recovery behavior a PN Diode has. And third, the body diode is a parasitic effect of building a MOSFET, and therefore it is not an optimized device. Furthermore,

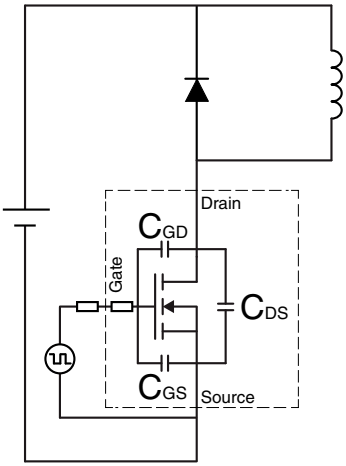

Figure 2.16: Circuit for transient analysis of a MOSFET driving an inductive load.

among the important guidelines when building a switching device is to maximize the figure of merit $\frac{V_B^2}{R_{DS(on)}}$ [2], and therefore the channel is constructed as thin as possible, with a heavily doped P+ side to ground the parasitic BJT of the MOSFET with a low ohmic connection. Both actions do not contribute to diode characteristics, and on the contrary, produce accentuated snappiness [10]. However, in SiC modules several devices do not include the Schottky diode as synchronous rectification is possible.

- Transient Characteristics

  The switching behavior of the MOSFET in ideal conditions is defined by its electron mobility and its electron saturation velocity [10]. But the frequency limit calculated in ideal conditions is not achievable in practice because of the MOSFET parasitic capacitances, which need to be charged and discharged in order to change the state of the MOSFET (hence they dominate its switching behavior). To describe the MOSFET transient behavior, the circuit in Fig. 2.16 will be employed. Important remark is that in datasheets these capacitances are described differently, as they are provided from direct measurements between terminals of the device. The datasheet defined capacitances are the input capacitance $C_{iss} = C_{GS} + C_{GD}$, the output capacitance $C_{oss} = C_{GD} + C_{DS}$ and the reverse transfer capacitance $C_{RSS} = C_{GD}$. However from them, all capacitances can be determined.

  The corresponding turn-on and turn-off events based on the circuit in Fig. 2.16 can be found in Fig. 2.17. Both events are separated in 5 sections, which are described as follows:

  Turn-on transient:

- Section 1 $t \in [t_0, t_1]$: The V_{GS} turn-on voltage is set on the gate at t_0, and therefore a current flows in the direction of the capacitance C_{iss}, which is essentially dominated by C_{GS} at this stage. The capacitance C_{GS} starts accumulating charge and its voltage starts rising exponentially with a time-constant $\tau = R_G C_{iss}$ where R_G is the total gate resistance. No changes occur in the MOSFET at this stage.
- Section 2 $t \in [t_1, t_2]$: The voltage V_{GS} reached the threshold voltage, and therefore a channel is built in the MOSFET, and it starts conducting. During this stage, since the MOSFET V_{GS} is still small, and the voltage V_{DS} is still the blocking voltage, the MOSFET is in pinch-off state. In this stage since the voltage V_{DS} stays constant, the depletion region is still the same size and hence the internal capacitances do not change. In other words, V_{GS} keeps charging with the same time constant $\tau = R_G C_{iss}$. During this stage the diode current commutates to the MOSFET. The drain current also carries the transient reverse recovery current of the diode turning off.
- Section 3 $t \in [t_2, t_3]$: As the opposite diode does not conduct anymore, it can build a depletion region and start blocking voltage. This unclamps the MOSFET from the blocking voltage, which starts to drop accordingly. This starts decreasing the depletion region on the MOSFET, increasing the variable capacitances C_{GD} and C_{DS}. This increase in capacitance translates on a plateau in the gate voltage, as in order to drop the forward voltage V_{DS}, C_{GD} must first be charged.
- Section 4 $t \in [t_3, t_4]$: Since C_{iss} stops changing as V_{DS} reaches single digits, now V_{GS} continues increasing until reaching V_{gg}, hence dropping V_{DS} slightly in the process and reaching the nominal $R_{DS(on)}$.
- Section 5 $t > t_4$: Now the MOSFET reached steady state characteristics, hence it is in turn-on state.

Turn-off transient:

- Section 1 $t \in [t_0, t_1]$: The V_{GS} turn-off voltage is set on the gate at t_0. Hence the device increases its resistance slightly, and therefore the voltage V_{DS} increases accordingly.
- Section 2 $t \in [t_1, t_2]$: The voltage V_{DS} surpasses the $V_{GS} - V_{TH}$ condition, and the MOSFET enters in pinch-off mode. The voltage V_{DS} starts rising, which means that V_{GD} must discharge accordingly to comply with $V_{DS} + V_{SG} + V_{GD} = 0$. Therefore, the voltage V_{GS} rests in the millers-plateau.
- Section 3 $t \in [t_2, t_3]$: As the MOSFET voltage reaches the DC-Link voltage, the capacitance C_{GD} stops varying and its voltage reaches its end value. At the same time, the opposite diode stops blocking and can start to carry current. In this stage, the current is commutates from the MOSFET to the diode. At the maximum di/dt point, the maximum overvoltage value is observed, which is a result of the parasitic inductances in the circuit. Finally V_{GS} reaches the threshold voltage.
- Section 4 $t \in [t_3, t_4]$: The MOSFET stops conducting. So now the C_{GS} capacitor discharges at the same rate $\tau = R_G C_{iss}$ due to the turn-off voltage that is set on the gate pin.

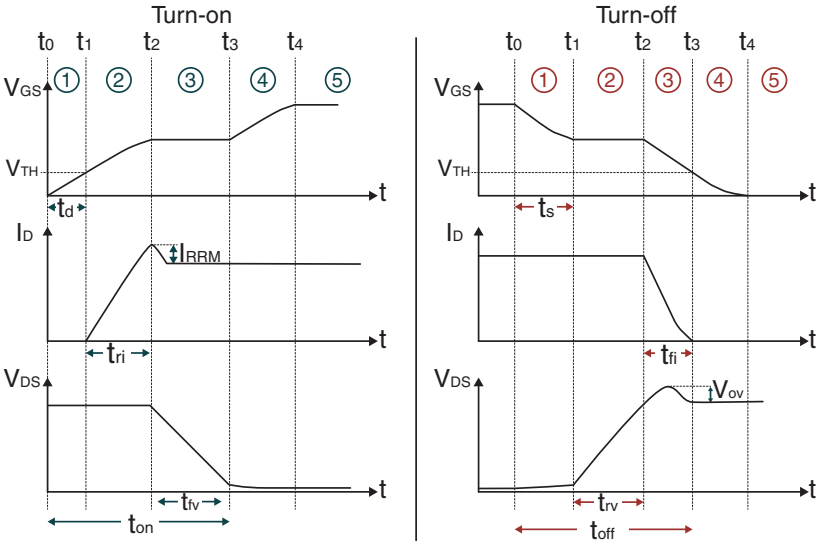

Figure 2.17: Switching curves and time definitions of the turn-on and turn-off transients of the MOSFET.

- Section 5 $t > t_4$: Now the MOSFET reached steady state, hence it is in turn-off state.

These stages define the switching behavior of the MOSFET, and will be used to cement the measurement definitions that are to come in the next chapter. Device switching losses occur in stages 2 and 3, and they will be an important constraint limiting the maximum switching frequency.

In summary, the SiC planar MOSFET is capable of high blocking voltages, with very low $R_{DS(on)}$ resistance and smaller parasitic capacitances than its silicon-based counterpart. Furthermore, its capability of synchronous rectification adds further capability of loss reduction, improving overall efficiency. However, as the channel mobility got better over the years, and the reliability of the gate oxide improved, the SiC trench MOSFET was introduced again as a device design possibility, hitting off-the-shelf market devices in 2014. Nonetheless, several considerations and some compromises had to be made in order to make this device a reality.

The SiC Trench MOSFET

The SiC trench MOSFET gets its name from its burrowed gate, which is within the crystal. In this case, the channel is made vertically, but presents smaller $R_{DS(on)}$ resistance in comparison with the planar variant as the effect of the accumulation resistance that occurs just below the gate on the planar structure does not exist in the trench [10]. Additionally, since the channel is now made

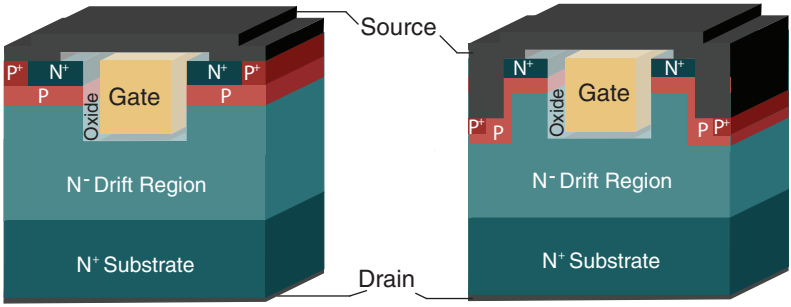

Figure 2.18: Trench MOSFET semiconductor structures. Left: Standard trench structure. Right: Double trench structure.

vertically, it is easier to control its thickness as it is grown by epitaxy layers. The traditional configuration of the trench MOSFET is presented in Fig. 2.18. However, its implementation usually also features a p-doped semiconductor below the gate (not in the picture) to protect it from high electric fields. To overcome the problems of the high electric field, the double trench configuration was introduced. In it, the highest electric field occurs below the p-type trenches on the sides, protecting the gate from high electric fields (see also Fig- 2.18).

The double trench configuration was the first solution to be implemented in commercial silicon carbide MOSFETs, and was introduced in the 3rd generation of Rohm MOSFETs devices [35]. In it, it is also shown how the on-resistance is halved when compared to their second generation, which is planar. This is to be expected as the channel resistance dominates in devices under 1200 V, and it gets reduced in the trench variant. The device also presents smaller input capacitance, which reduces switching losses. All these improvements come at the cost of a smaller short circuit withstand time, which is halved when compared with their planar design, and it is estimated to be around 5µs. However, there are other SiC trench MOSFETs in the market. Infineon MOSFETs are trench devices [50], but unlike traditional designs they feature a non-symmetric device structure that is specially designed to balance the C_{GD}/C_{GS} ratio to prevent parasitic turn-on. Additionally, it uses a thicker channel that is built on a particular face of the crystal structure, highly improving its mobility, and therefore achieving reasonable $R_{DS(on)}$ values.

But then. What really makes SiC-MOSFETs special? The answer is rooted, as in SiC diodes, in its $R_{DS(on)}$ resistance, which rivals Si bipolar loss without having to use conductivity modulation. This allows the SiC-MOSFET to block high voltages with comparatively equal conduction losses as a Si-IGBT, but without conductivity modulation issues that hurt transient energy losses. Additionally, the smaller parasitic capacitances translate in shorter switching times. Hence sectors 2 and 3 (Fig. 2.17) of the switching events get shorter, allowing higher switching frequency for the same loss, or improving efficiency in trading off switching frequency.

2.4 Market of Silicon Carbide Devices

The theory behind the behavior of silicon carbide devices has been presented, but in order to get the whole picture of the state of art of these devices, it is crucial to understand the market evolution that device manufacturers have developed over the years. This insight enables the prediction of future devices, market trends and industry focus, which can provide interesting insights into market penetration and readiness of SiC devices, complimenting theoretical analysis.

To this end, three different market research studies have been considered over the years 2015, 2017 and 2019. Over 1000 datasheets have been considered and its main results are presented in the following sections.

Disclaimer: In this study, only devices that were confirmed to be in mass production stage or/and have definitive datasheets have been included. The reason for this decision is that there are several manufacturers in industry that have preliminary datasheets since years without ever launching the devices into the market. And on the other hand there are manufacturers that sell devices while their datasheets still are presented as preliminary or target. Hence, if the product is not confirmed to be in mass production and its datasheet was presented as preliminary/target, then the product was not included as active.

2.4.1 Discrete SiC Devices

The landscape of discrete semiconductors has developed drastically in the last decade. As previously presented in Fig. 2.5, SiC diodes exists since the beginning of the XXI century, but market off-the-shelf SiC active switches belong mostly to this decade, with the exception of the JFET. However, this device was rapidly replaced by the MOSFET, which is the dominant SiC active switch on the market as of 2020. The main results of the market study of off-the-shelf SiC devices are presented in Fig. 2.19.

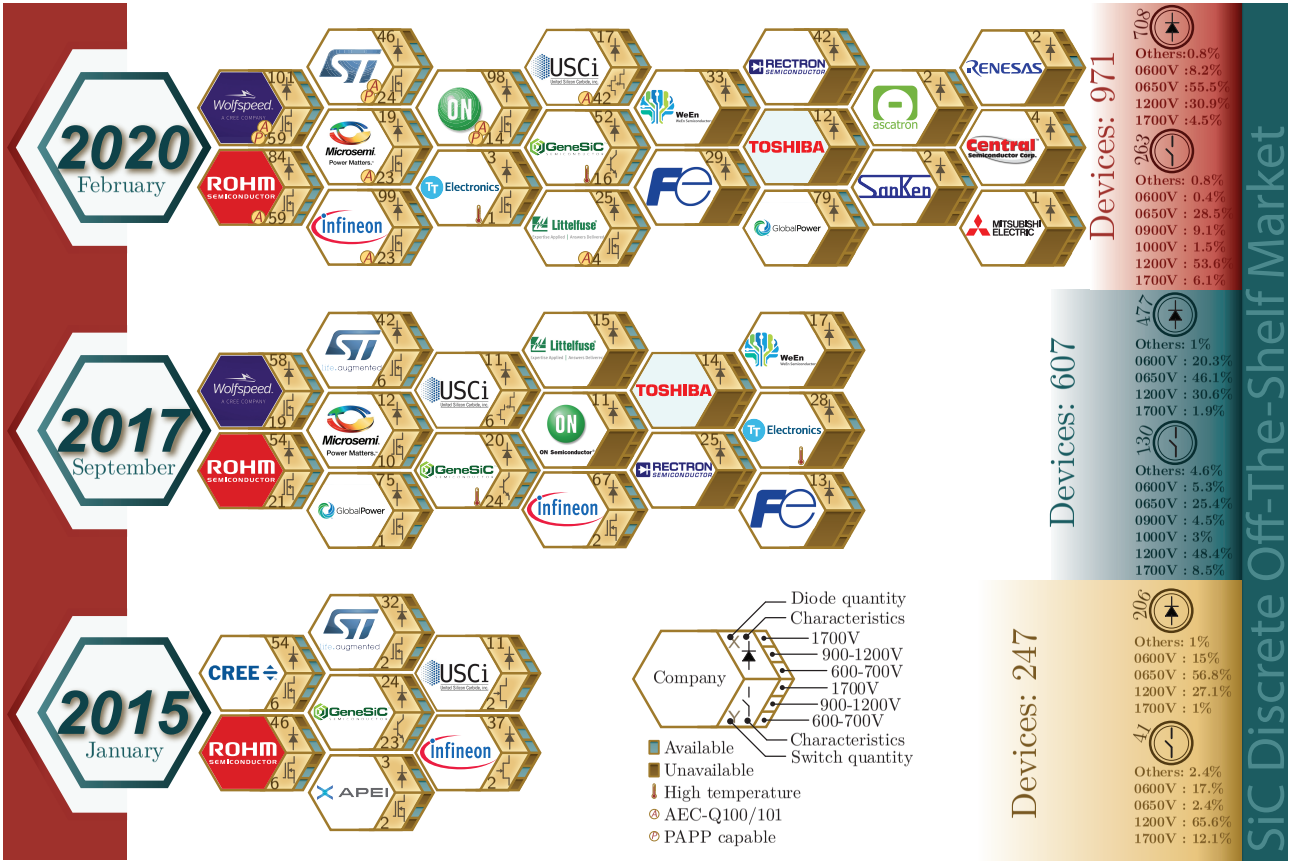

Figure 2.19: Evolution of the market and devices of discrete SiC semiconductors over 2015, 2017 and 2020, based on extensive online research.

In Fig. 2.19 it can be observed that in just the time-span of 5 years, the companies working in the silicon carbide business have more than doubled, and devices have quadrupled so far. It can also be observed that in 2015 the majority of SiC switches were rated in the 1200 V range. A possible reason of this effect is that the 1200 V is a reasonable trade-off between blocking voltage and $R_{DS(on)}$ resistance. At lower voltages the $R_{DS(on)}$ resistance is dominated by the channel instead of the drift region, and with the low mobilities observed back then, they were not as attractive to showcase SiC characteristics. Additionally, at the time renewables were the main application in which silicon carbide devices provided an advantage, and to that application 1200 V devices were more attractive than the 600 V counterparts. Nowadays, an increased amount of 650 V switching devices has arrived to the market, being almost 1/3 of the total market offer. The main suspected reason of this behavior is that the SiC industry is right now being driven by the automotive industry demand instead of renewables, and to that application, 600-900 V devices are required. This market driving factor can also be observed in the certifications major SiC developing companies have pursued. All big players in 2020 have applied for the AEC-Q100/101[7] certification for some of their devices. Some of them also offer PAPP compatible devices, which is a screening process implemented in the automotive industry to ensure reliability.

Regarding device development, it can be observed that although in 2015 several SiC switches from heavy-weight manufacturers existed, in 2020 it is clear that the market selected a structure. The SiC-MOSFET is currently the dominating active SiC device structure, and most companies that were not developing MOSFETs at the time, are doing so now. Infineon is actively developing SiC-MOSFETs and Genesic is also switching to SiC MOSFETs as their main switching product, which leaves United Silicon Carbide (USCi) as the only manufacturer that is sticking to a different switch scheme as their main SiC switching product in their portfolio.

On the other hand, in Fig. 2.20 a summary of the main packages used in discrete SiC devices is presented, and although the image source is from 2018, it has not changed so far. In SiC devices, because of its high switching speed, parasitic inductances in the devices can cause dangerous overvoltages that were not a problem in silicon. Therefore new configurations appeared in the market to minimize the effects of parasitic inductances. 4 leg packages such as the TO-247-4 were used to provide a kelvin source in the driving circuit, hence providing a low inductive path for the gate circuit. Also packages with multiple pins such as the TO-263-7 are used to drive the current through multiple pins to further reduce the effective parasitic stray inductance of the device. However, these improvements are considered incremental, and no additional changes have been observed in the discrete packaging sector.

Regarding high temperature devices, the main companies producing high temperature devices are TT-electronics and Cissoid[8]. However, both companies operate mostly by offering tailored solutions for the respective applications, and therefore have reduced their off-the-shelf device offer. Genesic also has high temperature devices, but they have not changed since 2015, and seems to be

[7] AEC is the Automotive Electronics Council and it has the purpose of establishing common part-qualification and quality-system standards. The referred standards are AEC-Q100: "Failure Mechanism Based Stress Test Qualification For Integrated Circuits" and AEC-Q101: "Failure Mechanism Based Stress Test Qualification For Discrete Semiconductors"

[8] Cissoid was not mentioned in this study as they do not have off-the-shelf silicon carbide parts available

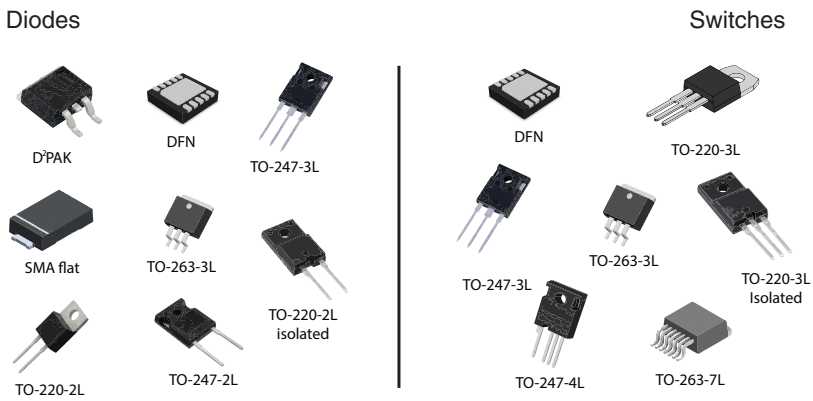

Figure 2.20: Typical discrete device packages

focusing in their transition to SiC-MOSFET devices.

2.4.2 SiC Modules

As previously mentioned, SiC devices present high current density, higher switching speed, lower overall losses and high temperature withstand capability when compared to silicon devices. However, to take advantage of these characteristics, an optimized package design must be provided. Minimization of stray inductance, thermal matching of structural components and semiconductors, and balanced parallel behavior of dies must be provided, and to that end power modules are the clearest choice to tap into the potentials of this technology for high power applications. A thorough market study of off-the-shelf full SiC modules has also been conducted, and its result summary is presented in Figs. 2.21 and 2.22.

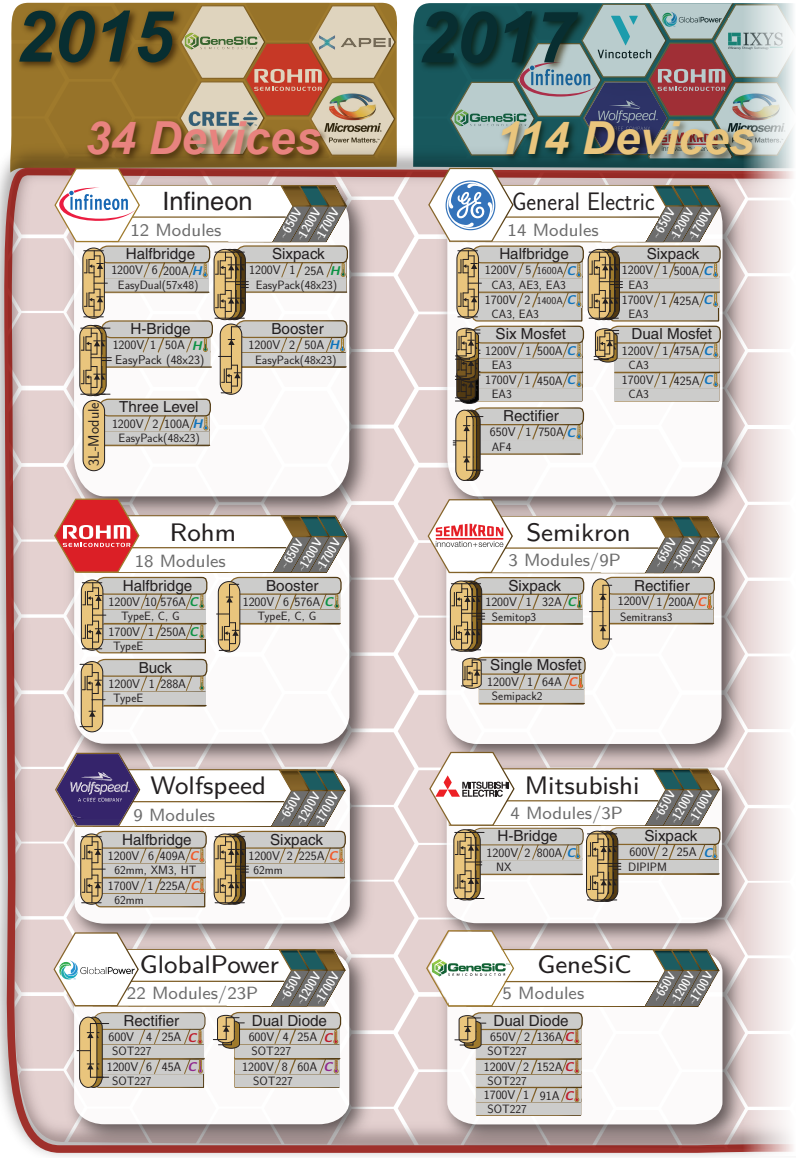

Figure 2.21: Market of off-the-shelf full-SiC Modules, Fig. 1/2. Based on extensive online research. If available, the current at the highest operating temperature was preferred.

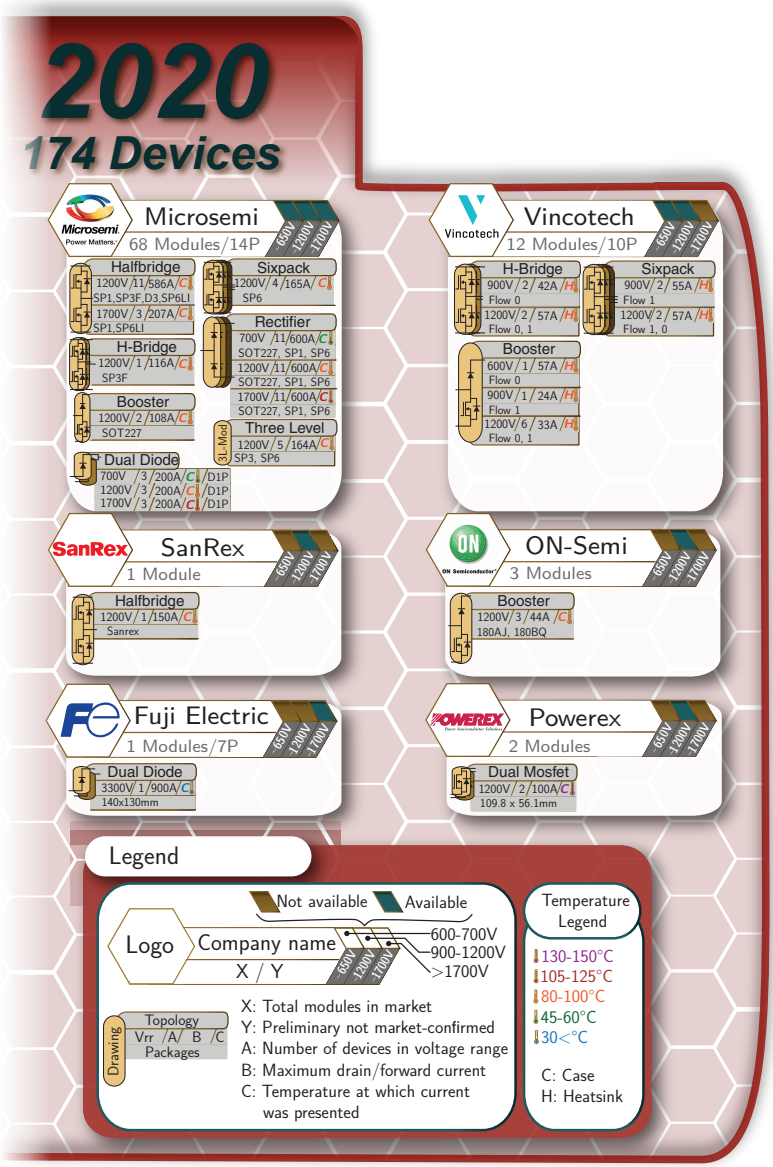

Figure 2.22: Market of off-the-shelf full-SiC Modules, Fig. 2/2. Based on extensive online research. If available, the current at the highest operating temperature was preferred. The temperature legend indicates a range in which the nominal current was provided by the manufacturer.

From Figs. 2.21 and 2.22, it can be observed that there is an astonishing development of module options in comparison with 2015, where only halfbridge, six-pack and single devices in SOT-227 packages were available. Before 2014, SiC modules were a technology that had to convince manufacturers to opt for the technology, and hence retrofitting was a high priority, making standard packaging solutions preferred. Additionally, the cost of silicon carbide wafers was (and still is) high, thus industry opted for same current ratings (therefore using less material) instead of showcasing higher rated currents for the same package. In other words SiC modules were made to be retrofit-capable while providing high-frequency capability and lower loss in the same form factor a Si module would use in the same application. Nowadays it is still a focus of manufacturers to convince customers to opt for SiC, but as there are already SiC devices on the market of power converters, device manufacturers can now direct research time in making devices that do not use standard packaging to obtain additional performance.

However, this increase in device offer has not been equal among all voltage ranges. Up to 2017 there were no modules in the 600 V range other than single devices in the SOT-227 package. Today there are several, although most of them are SiC diode modules. The biggest growth has occurred in the 1200 V range, which now presents the highest number of topologies regarding SiC.

In the 1700 V range, only Wolfspeed, Rohm, General electric and Microsemi present SiC modules with active switches on the market, and although it is expected that all manufacturers use planar devices in this voltage range, only Wolfspeed and Rohm are confirmed to do so. General Electric joined late, but now presents devices with outstanding current driving capability. Note that the high current driving modules from GE are the big-sized modules (133x90x29 mm^3). Their smaller versions of the half-bridge (89x51x25 mm^3) do present similar current ratings as the competition (425 A-1700 V).

Now in 2020, several module designs are still based on the classic standard packages that silicon IGBTs have been using until now, such as the 62mm and the econodual format among others. Nonetheless, several other interesting alternatives have appeared on the market (Fig. 2.23). Starting with Wolfspeed, they offer two particular SiC module packages specially designed for SiC. The HM2 package is rather old, as it dates from 2014 when APEI and Cree were different companies. However, this device can operate at junction temperatures of 175°C and used an AlSiC baseplate and Si_3N_4 insulator specifically designed for reliable thermal cycling capability. In the XM3, the design overlaps the DC-Link plates as much as possible, hence reducing total circuit stray inductance. It also presents very low inner stray inductance (6.2 nH) and can operate at a junction temperature of 175°C. Both of these solutions are only available in the 1200 V range. On the other hand, Infineon presents compact packages based on SiC trench MOSFETs. These modules are baseplate-less and feature pressfit pins, simplifying design when high power density is required. Microsemi also introduced a new package in the recent past, the SP6LI package, which while having the same dimensions of a 62mm module, presents a remarkably small stray inductance of (2.9 nH). Additionally, this module package is also present for 1700 V devices, being among the best package options in this voltage range at the moment. Next are the proprietary modules from General Electric, featuring very high current capability and allegedly ultra low stray inductance, but actual values have not been found as datasheets are not public and only brochures

have been found. On the other hand, Fuji has developed the L1, L2 and L3 packages, which although have still not been seen in the market, they will be able to operate reliably at junction temperatures of 200°C. Additionally, they eliminated wire bonds using direct pins to the semiconductor to minimize stray inductance effects. Next, Mitsubishi Electric presented their NX package, which inherently parallels modules while significantly reducing footprint. Rohm has further improved traditional packages, reducing total stray inductance to 10 nH in a package that is easily retrofittable in classic silicon-based converter designs. Finally, Sanrex presents an ultrathin halfbridge package for 1200 V designs with high power density goals. These are only a handful of interesting examples, and it is expected that Silicon Carbide particular characteristics will continue driving device packaging development in the near future.

Figure 2.23: Remarkable module packages in 2020.

As it can be observed, SiC device development has been focusing in the 1200 V area, with some exceptions reaching the 1700 V range. An important exception in the 650 V range must be made to mention the 650 V-100 A SiC modules that ST-micro is manufacturing for Tesla motors, particularly for the model 3. These devices will be manufactured in great numbers to be used in the main inverter of the car but were not considered in this study as they are not off-the-shelf devices.

2.5 Applications

Finally, to understand the whole picture of the silicon carbide industry, a small overview of the applications that benefit of this technology has been performed. Essentially, these applications highly value a mix of the following characteristics:

- High efficiency
- High power density
- High switching frequency
- Harsh enviroment operation

However, in order for the application to use SiC, these characteristics need to be highly regarded for the application, as the advantages to be obtained from SiC need to be attractive despite their higher power semiconductor costs. A summary of some of the most prominent applications benefiting from the technology can be found in Fig. 2.24.

- Automotive

  Electric vehicle components using SiC devices were among the first uses of the semiconductors to reach market applications. An electric car highly benefits from both high efficiency and power density, as both impact the car distance driving range, which is among the most important figures of merit of an electric car. Among the first products, Toyota developed a power converter unit for hybrid electric cars based on SiC [51]. In 2014 the Toyota Prius battery charger followed - a 6.1 kW converter from cooperative development with CREE and APEI that reached 95% efficiency while operated at 200 kHz and featuring a power density of 3.8 kW/kg [52]. In the more recent past John Deere showcased in October 2018 the second iteration of their SiC inverter for their backhoes [53]. This 200 kW 1050 V_{DC} inverter allowed the use of a single coolant circuit (as the devices can run hotter), and therefore saved additional weight in the overall design. Finally, Tesla motors moved away of their paralleled discrete IGBTs to using 24 SiC-MOSFET modules provided by ST-micro in the main inverter [54], which had to ramp production and ensure SiC wafer availability with both Wolfspeed and SiCrystal (Rohm). This driving industry could ramp production to the point of mainstreaming silicon carbide in this application, reducing its bulk price for other applications as well.

- Solar Photovoltaics

  Solar PV power converters were the main target application industry before electric vehicles. The main advantage PV-solar inverters gain from SiC semiconductors is high efficiency, as a single won efficiency point means high

dividends over years of operation [33]. This improvement is perceived as a requirement for next-generation PV converters [55] in order to improve their market penetration. Additionally, the cost of power converters in large scale solar plants is not the most significant part when compared with the overall cost of a solar farm project, and therefore the extra spending on the converter for improved efficiency can be justified.

But SiC does not only provide efficiency improvements to PV applications. The use of high switching frequency reduces passive component requirements, and as seen in [56], this can reduce the bill of materials (BOM) cost up to 15%. The final result is one fifth of the weight of a Silicon converter with the same characteristics, higher efficiency (one point more than the Si-IGBT competitor) and a higher power density (1.5 kW/kg rather than 0.3 kW/kg).It should be noted that the main BOM costs are enclosure, inductors and heatsinks rather than the semiconductors. Thus, even though the SiC switch is 3-5 times more expensive than the Si alternative, the final BOM cost reduces.

Going to rooftop applications, the weight and volume reduction simplifies installation, and a reduction in space is always welcomed when installing equipment at a domestic level. These benefits, although not technical, are along the economic benefits also important to the residents when deciding for installing rooftop setups.

As a large scale power converter example, the most prominent is the 1 MW, 99% effiecient SiC solar inverter from General Electric, called LV5+ [57]. This converter is also being actively employed in the second stage of the solar park Mohammed bin Rashid Al Maktoum in Dubai [58], as a part of a 200 MW expansion to the first stage of the project.

Alternatively, and for smaller solar plants, the 250 kW string inverter SG250HX from Sungrow employs infineon CoolSiC MOSFET modules [59], featuring 99% efficiency and power density of 1 kW/Lt.

- Traction

  Converters for traction applications were also among the first applications to consider this technology, as they have also high efficiency and high power density as a priority. In traction applications, the connection with the grid is almost always present, hence not being necessary to provide energy storage. Some example market applications of SiC technology in traction are the use of full-SiC modules for the Shinkansen bullet train [60], in which a 305 kW inverter for the four traction motors were implemented. Another example is the case of Bombardier's MITRAC TC1500 traction inverter, which was used in their C20 vehicles to reduce energy consumption by 35% [61].

- Aerospace

  Aerospace applications are an obvious target for SiC technology, as the weight and volume reductions are priorities in this field. A lighter plane provides advantages in fuel consumption and the higher switching frequency not only enables power density improvements, but also simplifies the coupling with onboard 400 Hz grids.

  Another important factor is the resilience of SiC switches against radiation [1]. Thanks to the wide energy bandgap of the material radiation effects must provide more energy to generate non-designed effects in the material, being more resilient than silicon devices for high altitude operation.

However, big commercial-flight airplanes are far from reach, being the biggest electric plane to ever fly a 9 seater plus pilot [62], as competing with turbine propulsion and fuel energy density is a challenging topic. Electric aircraft nowadays is reserved for small aircraft, typically propeller based or in auxiliary equipment for bigger aircraft. As market examples, there is the MagniX magniDrive [63], a 170 kW 98.8% efficient water cooled SiC-based motor drive for aerospace applications. Additionally, two auxiliary equipment products for aerospace applications from GE aviation are shown as examples in Fig. 2.24 [64].

- Uninterruptible Power Supply (UPS)

  In high power UPS devices, the primary power path is managed through the power converter and therefore the efficiency of the system is of high importance as these devices are rarely off. Additionally, these systems require an isolated design path to the power storage units, which is something that high-frequency DC/DC converters can help with.

  In UPS systems, among the interesting prototypes a 10 kW full-SiC power converter was presented in [65]. The project from Rohm and Fraunhofer ISE contemplated the design of a low voltage converter MNPC converter for UPS, using a 0 Flow Vincotech module. The final design was 23 x 21 x 10 cm^3. Nonetheless, nowadays there are already some market examples based on SiC. Toshiba and Fuji, [66,67] feature high performance UPS devices presenting SiC-based solutions. Toshiba presents a full-SiC based solution featuring 98% efficiency over wide load ranges while being more compact than their silicon counterparts. On the other hand, Fuji presents a UPS using hybrid modules, peaking at a 97.2% efficiency.

- High Voltage/Medium voltage

  Finally, also an important application area could be be high or medium voltage power converters. The higher critical electric field should allow these devices to reach high blocking voltages. In literature, already over 10 kV SiC based blocking devices have been observed, and therefore, once these devices reach market maturity, will allow their use in medium voltage applications without the need of serialization or step-up transformers. There are currently no industrial medium or high voltage converter examples in the market. However, a prototype of a 10 kV 100 kVA statcom from Fraunhofer institute is presented [68], demonstrating the potential of SiC devices in medium voltage applications.

- Others

  There are several other application areas that would, and do benefit from the use of silicon carbide devices, but their importance and market share is not substantially significative. Examples of these applications are induction heating, PFC, medical and oil drilling applications, which already do benefit either from its high frequency capability or high temperature operation, but their influence in the market is less significative. Wind turbines, general purpose industrial electric drives, and high speed drives would also benefit from the properties of silicon carbide, but their perceived benefits versus additional cost is not as clear. Finally, military applications do highly benefit from this technology, as improved material ruggedness, high temperature operation, radiation resilience and high power density are very attractive characteristics for this application. However, no information of market applications has been

found, being more hinted by SiC device manufacturers than field applications featuring the technology.

A summary of the mentioned application prototypes is summarized in Fig. 2.24 at the end of this chapter.

Figure 2.24: Market examples/industry grade prototypes of SiC-based converters in determined applications.

2.6 Summary

In the present chapter, the main characteristics of the devices relevant to this thesis have been presented and their market state and recent evolution has been discussed. Silicon carbide has attracted increased interest from the research community, as it enables higher blocking voltage devices with thinner layers of material, and presents more current driving capability with less die area, while

presenting outstanding thermal characteristics. This brings SiC unipolar devices into Silicon bipolar device territory. The evolution of this material and its irruption into the market has been frenetic, and in the last five years an exponential growth on both discrete and module device options has been observed. However, the corresponding consequences of using highly current dense unipolar devices while switching at high frequencies sets requirements of its own. Hence, it remains to be studied how these material advantages translate into safe and reliable converter characteristics, and how these fare against classic silicon-based solutions.

3 Device Characterization of the 1700 V, 250 A SiC Module

This chapter introduces the reader to the SiC-MOSFET module that was selected to build the three-phase two level inverter demonstrator. First an introduction to device selection criteria is detailed, followed by a description of the experiments that were performed for its characterization. Signal parameter definitions, test-bench descriptions and used probes and measurement instruments that were used to electrically characterize these devices are presented. Finally, the results of both the single module and its parallel-connected configuration are presented and discussed, and a summary of the main conclusions of the corresponding results is performed.

3.1 Converter Requirements, Module Requirements and Device Selection

As presented in Chapter 1, to achieve the main objective of this work a three-phase two level SiC-based converter for 690 V_{ll} grids in the 230-300 kVA range (272-350 A_{peak} phase current range) is to be design and implemented. To achieve this goal without serial connection of devices, 1700 V devices are to be used, as the DC-Link voltage of such a converter needs to be nominally over 1000 V to be able to modulate the required voltage levels with full control capability for every angle of the $\alpha\beta$ (Clark transform) grid voltage vector. In this particular case, the defined nominal DC-Link voltage is V_{DC} = 1080 V.

At the end of 2017, a market study was performed in order to obtain information regarding the availability of 1700 V SiC based modules. From this study, device candidates were selected with the objective to characterize their behavior and assess their suitability to develop the aforementioned converter. In the market at the time of selecting devices, there were only two 1700 V modules capable of handling high current; the Wolfspeed CAS300M17BM2 [69] and the Rohm BSM250D17P2E004 [15] (known at the time as BSM00015A). These two half-bridge modules can be found in Fig. 3.1, and their characteristics can be found in Table 3.1.

Both devices feature MOSFETs of planar structure, which is to be expected due to the higher electric field these devices need to withstand. Furthermore, until today, no hints have been found that could hint that Wolfspeed is interested in building trench devices. On the other hand, Rohm and Infineon already feature theirs on the market, but are reserved for 1200 V and below. Regarding the in-module parallel SiC Schottky diode, the Wolfspeed module is suspected to use a JBS diode, as Wolfspeed sells their modules with JBS diodes and discloses them as Schottky. On the other hand, ROHM has communicated to us that they use a classic Schottky diode structure for this module.

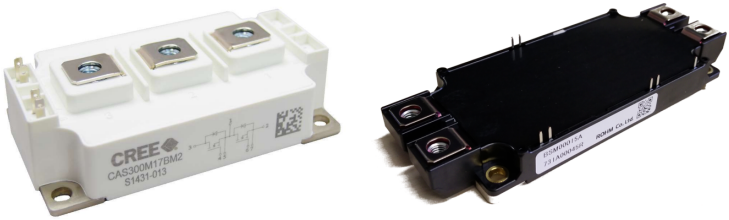

Figure 3.1: Left: Wolfspeed CAS300M17BM2 1700 V SiC module. Right: Rohm BSM250D17P2E004 (BSM00015A) 1700 V module.

Table 3.1: Datasheet based main characteristics of the presented full-SiC half-bridge modules.

	Rohm BSM250D17P2E004	Wolfspeed CAS300M17BM2
V_{DS}	1700 V	1700 V
I_D	250 A_{DC}@60°C	225 A_{DC}@90°C
L_S	13.3 nH	15 nH
$R_{DS(on)}$	8 mΩ	8 mΩ
$V_{GS(off)}$	[-2, 0] V	-5 V
$V_{GS(on)}$	18 V	20 V
$V_{GS(MAX)}$	[-6, 22] V	[-10, 25] V
V_{TH}	2.6 V	2.5 V
Q_G	1700 nC	1076 nC
$R_{G(int)}$	1.8 Ω	3.7 Ω
T_{jmax}	175°C	150°C

From Table 3.1 it can be observed that although the device ratings are similar, slight differences can be observed among manufacturers. For example, the Rohm module can be driven with 0 V turn-off voltage (although -2 V is recommended) and requires 18 V instead of 20 V to perform with its rated $R_{DS(on)}$ resistance. On the other hand, the Wolfspeed module presents a smaller gate charge, which should provide a theoretical advantage in switching time if not for its higher internal gate resistance. However, and although datasheet based switching times are similar, the provided data is not directly comparable as the datasheet disclosed characterization conditions for the double pulse tests of both manufacturers are not identical.

Additionally, it is clear from Table 3.1, that two devices in parallel will be required in order to be able to safely drive the required phase currents.

After due consideration, the Rohm BSM250D17P2E004 device was selected because of the following:

- Conservative manufacturer with focus on reliability [35, 70].
- Availability and fast delivery of samples.
- Slightly lower stray inductance than the competition at the time.

- Extensive datasheet data.
- Industry standard EconoDual package.

3.2 Characterization of the 1700 V, 250 A ROHM SiC-MOSFET Module

3.2.1 Introduction

As thorough as datasheets can be, device characterization is a crucial step of converter design. The need for characterization rises from the need of understanding the behavior of the devices in the operation points the converter is expected to perform aiming to predict its behavior, estimate its losses and define operation limits such as converter nominal current and switching frequency. Some of the disadvantages of relying only on provided datasheet values are the following:

- Datasheet used blocking voltages in several experiments are optimal for the module and usually are performed at close to half the nominal blocking voltage of the device. However this value can be different from the required for a particular application.
- Tabulated datasheet data offers information of the module parameters while usually measured in optimal conditions for the corresponding parameters (room temperature, small/big gate resistances, low circuit stray inductance, etc.).
- Most information regarding switching behavior is only referential. This is due to the fact that there are several independent variables in a switching event, from switching layout and gate unit, to operation points and temperature, and therefore the particular implementation of the application will usually differ from datasheet provided data.
- The presented results can be a statistical average of a batch of devices, or a measurement that includes a safe margin, as some datasheet provided data is assumed to be guaranteed by manufacturer. Therefore, datasheet provided information can differ from the characteristics of the batch under study.
- Engineering samples are likely to come along with preliminary/target datasheets. This means, they can lack data and can present unconfirmed or design-goal values instead of measured datapoints.
- Data of important parameters measured at different temperatures is typically limited.
- Short circuit data is scarce, and typically absent in datasheets.

Therefore, due all these reasons it is safe to state that datasheets do not provide the full picture of how a device behaves in a particular application and operation point. And therefore, a device characterization of the halfbridge SiC-MOSFET module was carried out in order to experimentally determine its static and dynamic characteristics. To determine the dynamic characteristics of the device, a Double Pulse Test (DPT) experiment has been performed, and for static characteristics, forward voltage measurements while driving DC-current through the

module have been carried out. To perform these experiments, a double pulse test testbench has been built, and for on-state measurements a DC-current source testbench has been used.

3.2.2 Transient Characterization by The Double Pulse Test (DPT) Testbench

The double pulse test event consists, as its name implies, in generating two voltage pulses through the gate unit on the gate of one of the switches in a module to turn-on the device twice and use these pulses to characterize its dynamic characteristics. To do so, the standard setup consists in a switch in series with an inductor, which is in parallel with a freewheeling diode. The used schematic for the characterization was built according to [71–73], and is depicted in Fig. 3.2 while its corresponding test waveforms are presented in Fig. 3.3. During the first pulse (switch is turned on) current flows through the switch and the load inductor, which is charged until reaching the desired test current. Then, at t_0, the device is turned off and turn-off characteristics are registered and processed. While off, the current in the load inductor freewheels through the diode, slightly decreasing. The decreasing current can be neglected as the time between t_0 and t_1 is short (µs range) by design to keep the current level as constant as possible. Then, at t_1 the MOSFET is turned on and both MOSFET turn-on characteristics and diode reverse recovery characteristics are measured at this point. Finally, at t_2, the MOSFET is turned off again, and afterwards the diode freewheels the current until it reaches 0. These experiments are repeated at different junction temperatures, which are set through heating the case temperature and waiting until homogeneous temperature distribution is achieved (ergo $T_C = T_J$). Afterwards, and after pulses have been performed, a wait time of approximately a minute between measurements has been left to ensure that the heat the pulses generated and the corresponding dissipation the current in the inductor generates while freewheeling through the diode to zero does not influence the next measurement. This is more than enough, considering that the slowest time constant of the transient thermal impedance model is in the tens of milliseconds range (see Table 4.3), and all current in the inductor is dissipated according to

$$V_f = L\frac{\Delta i_L}{\Delta t} \rightarrow \Delta t = L\frac{\Delta i_L}{V_f} \rightarrow \Delta t = 380\,\mu H\frac{250\,A}{2\,V} \approx 47.5\,ms \tag{3.1}$$

in approximately 50 ms, which is negligible against the minute of waiting time. However it was nonetheless confirmed that the temperature of the heatsink reading was on the setpoint at the beginning of a DPT event.

For the MOSFET, the main time-critical parameters to measure are turn-on delay time $t_{d(on)}$, turn-off delay time $t_{d(off)}$, current/voltage rise/fall times t_rx/t_fx, and turn-on/off energy E_{ON}/E_{OFF}. Additionally, the maximum MOSFET dv/dt and di/dt during both turn-on and turn-off transients were registered. These definitions are graphically presented in Fig. 3.4. Timing values are critical to define switching dead-times and compare the effects of different gate resistances. Energy values on the other hand, are key to simulate converter operation and determining nominal currents and switching frequency. Finally MOSFET dv/dt and di/dt values are important to assess EMI effects, estimate the risks of overvoltages, miller currents, crosstalk, and risks of MOSFET dv/dt failure mecha-

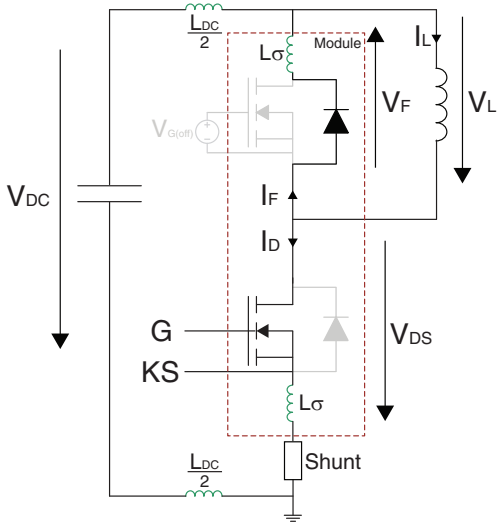

Figure 3.2: Implemented Double Pulse Test (DPT) schematic with parasitic inductances depicted in green. Probes assigned to the shown signals in this schematic are described in Table 3.4.

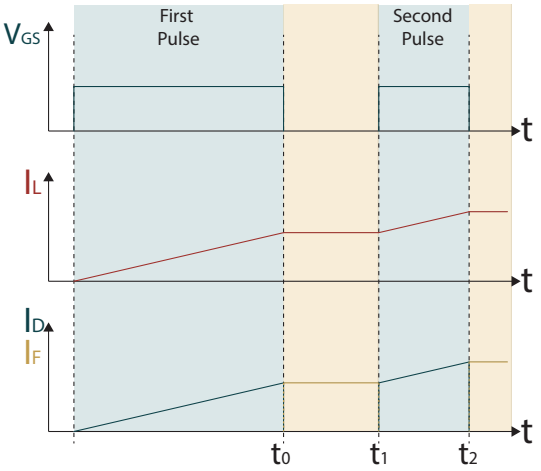

Figure 3.3: Double pulse test standard waveforms of the gate voltage V_{GS}, the inductor load current I_L, the MOSFET Drain current I_D and the diode forward current I_F.

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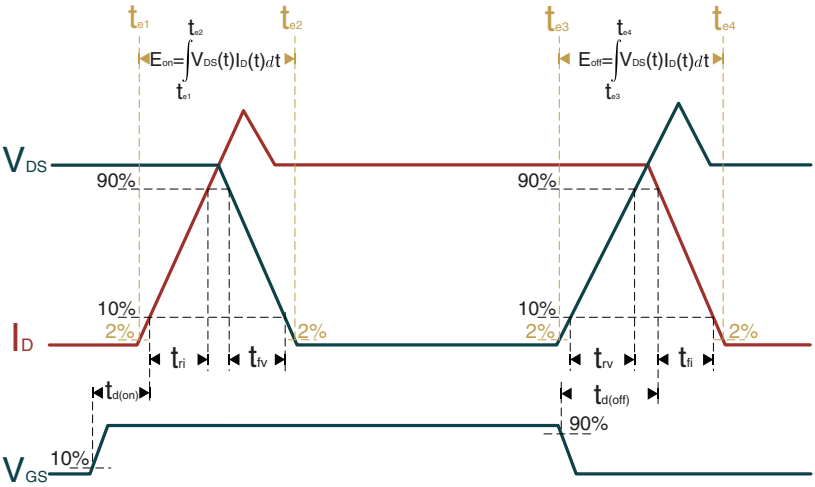


Figure 3.4: Simplified waveforms and main timing/energy definitions for the SiC-MOSFET characterization.

For the diode, the main time critical parameters are the reverse recovery energy E_{RR}, and the maximum dv/dt and di/dt during its turn-off transient. These definitions are graphically presented in Fig. 3.5. However, in contrast to what it has been observed in silicon diodes, as SiC diodes switch faster resonant modes due to parasitic elements are excited, generating oscillations that are big in relation to the medium value of the signal. This fact makes the detection of the 2% of I_{RMM} crossing challenging, as this event can be triggered by an oscillation and not by its average value, missing a significant portion of the accounted energy. Furthermore, the total reverse recovery energy is in the single milijoule units. Thus, it is particularly complex to measure this energy consistently for every measurement. To solve these issues, the maximum and minimum of every period of the oscillating signal were averaged, and the resulting points where exponentially fitted. This new curve is then used to determine the 2% of I_{RMM}. This method was preferred to other proposed alternatives as it allows to measure consistently through several rows of measurements, while not fixing the corresponding integration time. Additionally, when no oscillations are present, both methods are to arrive to the same result.

Testbench Construction

The DPT testbench was specifically constructed for the dynamic characterization of this device, and it can be found in Fig. 3.6. It is organized in trays from top to bottom as follows: 1) Measurement instruments and communications with external computer, 2) DC-Link, hotplate, Device Under Test (DUT) and control platform, 3) Voltage source and 4) Load inductor. In the same figure, a 3D model

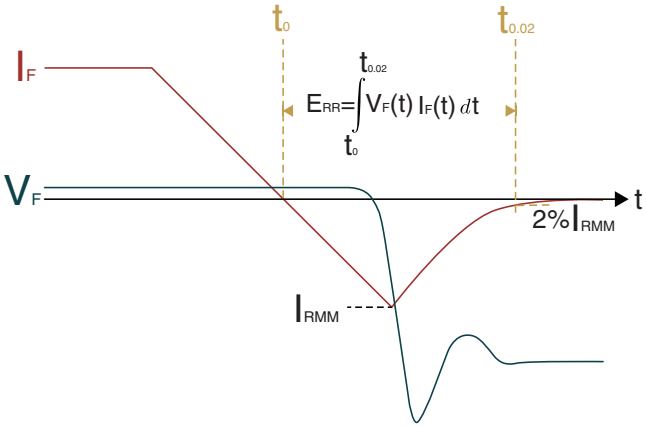


Figure 3.5: Simplified waveforms and main timing/energy definitions for the SiC-SBD characterization.

of 3rd tray with the DUT can be found, marking the main physical connection points. The corresponding schematic diagram is presented in Fig. 3.2. The gate signals and communications with the power source were handled inside the cabinet by the control unit, which is based in the Xilinx Zynq 7010 SoC and a control board developed by the TU-Dresden chair of power electronics. Additionally, both the oscilloscope and the control unit were connected to an external computer via ethernet through an optic fiber connection to ensure isolation between user and testbench as a safety precaution. The case temperature (and therefore, the junction temperature after the corresponding thermal time constants) can be adjusted through the hotplate, which consisted in a heatsink with a resistance array attached to its back and driven by a hysteresis controller which feedbacks the temperature through a PT100 temperature measurement probe.

The passive elements in charge of storing energy were the DC-Link capacitors and the load inductor of the circuit. The DC-Link is composed of five low inductive film-based 22 µF paralleled capacitors, which can be found along its corresponding data in Table 3.2. Due to their very low stray inductance, no decoupling capacitors have been used. The respective copper plate shape was simulated with INCA3D, to ensure low overall stray inductance, and its module terminals were bended as compromise to be able to connect the corresponding shunt resistor. The stray inductance observed from the MOSFET terminals was determined to be 40 nH, which would be equivalent of a DC-link stray inductance of L_{DC} = 26.7 nH. On the other hand, the load inductor is a custom designed air coil to avoid possible core saturation issues. Its value is of 380 µH, and its correct implementation was confirmed through measuring its impedance with an impedance meter. A summary of the testbench equipment can be found in Table 3.3.

a)

b)

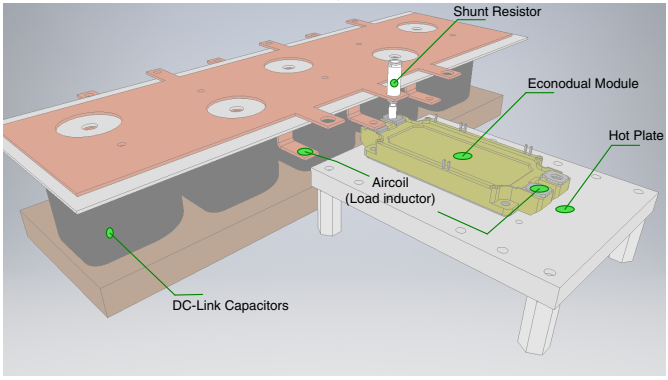


Figure 3.6: DPT testbench. a) Testbench cabinet separated into four sectors. 1) Measurement instruments & COMMs, 2) DUT, 3) Power source, 4) Aircoil. b) DUT cell 3D closeup, detailing connection points and the components of the switching cell.

Table 3.2: Capacitor characteristics.

Parameter	Value	Image
Part	FFVS6N0326K–	
Capacitance	22 µF	
Type	Film	
Max Voltage	1900 V_{DC}	
Max ESL	16 nH	
ESR	1.58 mΩ	

Table 3.3: Testbench equipment summary.

Testbench	
Oscilloscope	Lecroy Wavesurfer 24 Xs 200 MHz
Power Source	Iseg HPS 2 kV 150 mA (HPp)
Control Platform	Xilinx Zynq 7010 SoC
DC-Link	110 µF
Aircoil	380 µH
Hotplate	25 to 125°C

Probe Selection

Probe selection requires special consideration when measuring SiC devices, as different measurement probes typically present a tradeoff between current/-voltage range and bandwidth. In this case, voltages of over 1000 V had to be measured with high bandwidth while current measurements had to be in the kA range without sacrificing bandwidth. The minimum required bandwidth was therefore an important magnitude for probe selection purposes and it was calculated using the method proposed in [74], which approximates the behavior of the probe as a first order low pass filter. Hence, the bandwidth can be calculated as

$$B_w = \frac{0.35}{t_r} \tag{3.2}$$

in which t_r is the risetime/falltime of the fastest signal to measure in the system. Based on (3.2), and datasheet provided data [15] on the fastest registered risetime (30 ns), the minimum required bandwidth is 11.2 MHz. Therefore, all probes were selected to have at least 5 times the required bandwidth in order to have enough leeway to measure the fastest estimated signals along its spurious transient effects. The only exception is the Pearson current transformer, which is used to measure the current flowing through the load inductor I_L, which presents a risetime in the µs range and therefore does not have high bandwidth requirements.

For current measurement purposes, the best possible trade-off that could be found was the shunt resistor SSDN-414-01. Among its advantages, it presents a small layout, does not extend the switching path (hence providing low added

Table 3.4: Measurement probe information and corresponding measurement magnitudes.

	Probes
I_D	400 MHz Shunt Resistor SSDN-414-01
V_G	500 MHz Passive Probe LeCroy PP009
V_{KS}	500 MHz Passive Probe LeCroy PP008
V_{GS}	V_G - V_{KS}
V_{DS}	300 MHz Differential Probe PKM Bumblebee
I_L	20 MHz Current Transformer Pearson model 401
I_F	I_L - I_D
V_F	100 MHz Differential Probe Lecroy ADP305

circuit stray inductance), could handle 6 joules of maximum dissipated energy, and presented 400 MHz of bandwidth. This was the best option among the alternatives, as Hall-effect based sensors with high bandwidth could not measure more than 50 A, and the fastest Rogowski coils in the market, although capable of high currents, present around 30 MHz of bandwidth. The main disadvantage of the shunt resistor is that it cannot be used in continuous operation due to the energy dissipation limit. Additionally, since it is a coaxial connection, it grounds the oscilloscope where it is connected, a consideration that must be taken into account when using passive probes.

For voltage measurement purposes, the easiest solution that allows non-grounded high voltage measurements while providing acceptable bandwidth are differential voltage probes. The PMK Bumblebee probe has been selected as it presents 300 MHz bandwidth, while being able to measure voltages of +/- 2 kV_{DC} differential input voltage.

A summary of all the used probes, and their corresponding measured magnitudes referred to Fig. 3.2 is summarized in Table 3.4.

Probe Synchronization (Deskew)

Every measurement instrument becomes from a determined frequency, a low pass filter. This means, they present a dynamic that damps high frequency oscillations at a certain cut-off frequency. This low-pass filter behavior is also tightly related with its time constant, which is accountable for probe delay in analog measurement instruments. To that, digital delay due to A/D converter, amplification and processing must be added if there is any kind of in-probe signal processing, resulting in ultimate instance in a measurement that is delayed relative to the originating event. This is usually no problem for most classic measurements as these delays typically play a role at the single nanosecond digits and if the system time constants are orders of magnitude bigger in comparison, this effect becomes negligible. On the other hand, in digital systems where this is critical, all probes are measured by cables which are identically long, present the same delay and behavior, and are all triggered at once. Making the whole measurement delayed from the moment it happened, but not among probes.

In the case of silicon carbide (and WBG semiconductors in general), this is a non-negligible effect as transients in SiC modules can occur in the tens of nanosec-

onds. Therefore, since different probes measure different signals, achieving adequate probe syncing is important. This is specially critical to calculate energy, as a delay between the current signal and the voltage signal will change the overlapping of the curves, hence introducing error in the energy calculation.

To tackle this problem, several alternatives are proposed in literature. In [75], a summary of probe syncing methods for wide bandgap semicondutors is presented and it is summarized as follows:

1. Use a sync fixture to synchronize the channels.
2. Use the probe compensation output of the scope as a standard square waveform signal source for V/I alignment.
3. Replace the load inductor for a low inductance resistor and perform a pulse over it.
4. Use the voltage dip in the measured V_{DS} voltage to sync its maximum with the inductor voltage.

From the mentioned methods though, the first is only compatible with tektronics probes and oscilloscope. The second operates the probes too far from operation points as it uses the 5 V output of the oscilloscope and is discouraged by [75]. The third method proposes the usage of a low inductive resistor. This was tested with a Vishay low inductive film resistor, but it proved not to be useful as even very low inductive resistors present non-negligible parasitic inductance. This generates oscillations and different slewrates for both signals, hence difficulting the application of this sync method. Finally the fourth method based the synchronization in the V_{DS} voltage drop while turning on the device. However, this dip is not like in IGBTs, where the drop is relatively constant (see Fig. 3.31 for reference), and therefore this method was also found not to be completely reliable for SiC, as different measurement points gave result to slightly different delay correction values.

To avoid these issues, a variant of the fourth proposed measurement method was used, and this consisted in the usage of the parasitic inductance on the source of the MOSFET $L\sigma$. During current rise of the MOSFET at the turn-on event, the voltage over the stray inductance between the kelvin source and source pins is produced alone by the I_D current variation (through V_{GS} and the MOSFET transconductance). Therefore, the voltage drop over the stray inductance is: $V_{L_\sigma} = L_\sigma \frac{dI_D}{dt}$. Thus, by measuring the current I_D it is possible to reproduce the voltage over the stray inductance via software and then measure the delay between this virtual signal respective to the voltage provided by the differential probe by maximizing the cross correlation between both signals. The benefits of using cross-correlation lay on the fact that since it is necessary to estimate the stray inductance of the source terminal to get the signal, (as datasheet data provides the total stray inductance from DC+ to DC-, but not the stray inductance of the terminal) cross correlation provides the same outcome no matter if there is error in this parameter.

To provide an example, in Fig. 3.7, a simulated current signal is driven through a 6 nH inductor and a resistor in the 100 $\mu\Omega$ range, which is a worst case assumption for the resistance of the pin, (as a bigger resistance value would dominate the advertised $R_{DS(on)}$ resistance), and 11.6 ns of delay in the simulated measurement have been artificially added as delay transport.

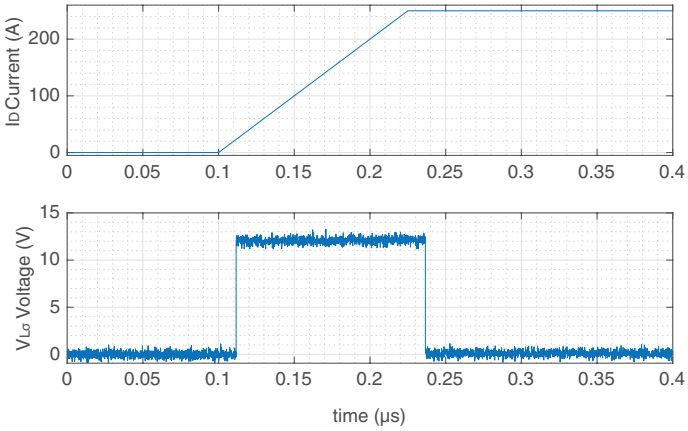


Figure 3.7: I_D and V_{L_σ} simulated example. In this example a stray inductance of V_{L_σ} = 6 nH, a pin resistance of 0.1 mΩ have been used, and a delay of 11.6 ns has been artificially introduced to simulate measurement delay in the voltage probe.

Reconstructing the voltage signal by using the current and two slightly off estimations of the stray inductance, the delay correction algorithm was performed and its results are presented in Fig. 3.8. In both cases the algorithm corrected the delay between signals correctly, demonstrating that the delay is eliminated correctly even if an error in the estimation of the parasitic stray inductance is performed.

Finally, the method was applied on real measured signals to correct the delay among the shunt resistor and the differential voltage probe. Results are presented in Fig. 3.9, and the total delay among probes was measured to be 8.3 ns, which is fairly close to the typical delay of the differential probe, which is 12 ns.

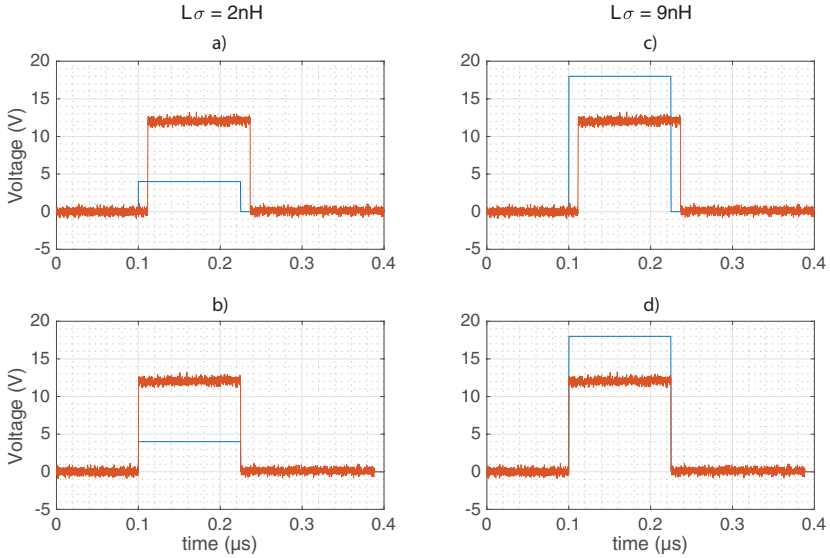


Figure 3.8: Sync method examples with different stray inductance estimation values. a) and b): Pre and post sync-corrected estimated(blue) and correct(orange) voltage signals by using an underestimated stray inductance value of 2 nH. c) and d): Pre and post sync-corrected estimated(blue) and correct(orange) voltage signals by using an overestimated stray inductance value of 9 nH.

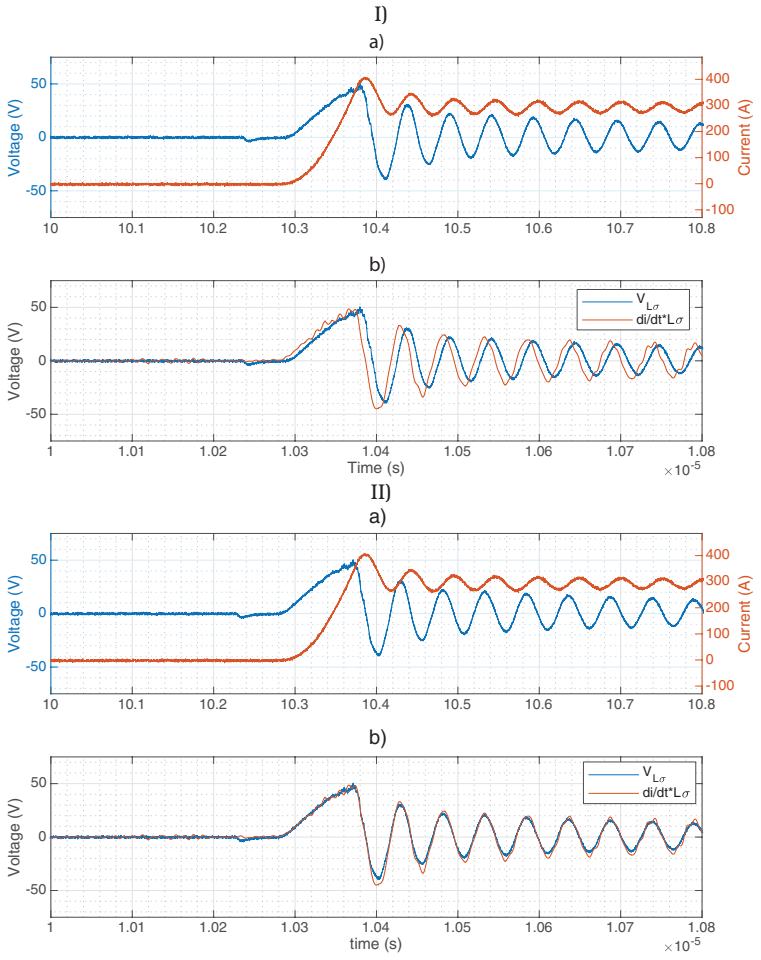


Figure 3.9: Sync method used in this work in action. a) Measured voltage and current of the source stray inductance. b) Comparison of the estimated voltage drop over the stray inductance by means of the measured current, and the measured voltage drop. I and II: Pre and post synchronization respectively.

3.2.3 On-state Characterization by High Current Source Testbench

On-state characteristics (forward and reverse characteristics) are mostly temperature dependent and do not depend on the circuit and operation points as dynamic characteristics do. In other words, as long as the driven voltages provided by the gate unit are the same, similar results should be obtained when compared with datasheet provided data, being among the possible differences mostly slight differences among device batches, and possible safeward margins that the manufacturer can include to guarantee device behavior as presented by datasheet curves. However, as previously mentioned, datasheet values only provide information of devices with limited information regarding temperature parameters, hence this measurement could provide additional insights into forward characteristic behavior.

In this case, two objectives were defined for on-state characterization:

- In single devices, an on-state characterization of the device has been performed in order to compare the curves with datasheet provided data to ensure that manufacturer's data used for simulation purposes has been adequate for device simulations.
- In parallel-connected devices, an analysis on current distribution during on-state has been performed in order to study on-state current sharing characteristics between the two modules.

In order to measure static characteristics, high DC currents are necessary to observe on-state voltage as both MOSFET and diode equivalent resistances are in the mΩ range. These DC currents should also be performed as fast current pulses, because if the module is in on-state for enough time, it will generate losses, changing the temperature conditions that were registered for the measurement. A curve tracer would be the ideal solution, as it performs the characterization of the devices with all considerations to avoid this self heating effect.

To perform the measurements, curve tracers and high current sources are commercially available. However, in this case a high current source testbench was already available in the laboratory, and therefore this system has been used. The testbench in Fig. 3.10, consists on two Si-IGBT full-bridges powering several MOSFET based synchronous rectifiers through two PCB transformers. Through this configuration, the setup is able to provide over 6 kA, and a maximum of 13.5 V output voltage. The module connection is straightforward, and its different measurement configurations are presented in Fig. 3.11.

As forward measurements do not have high bandwidth requirements, the probes for the DPT testbench could also be used. Therefore, the measurements were performed using the same hardware as in the corresponding DPT testbench. The shunt resistor and the PMK bumblebee differential probe in the 50:1 configuration (50 V) range was used. The measurement probes were described in Table. 3.4.

Therefore, the most important challenge in performing measurements with this testbench was to avoid or attenuate the effects of self heating: the dynamics of this testbench take between 1 and 3 ms to reach the reference current and this means that the device, depending on operation point, could heat up during this transient, altering the measurement conditions from which the results

Figure 3.10: High current source testbench cabinet used for forward characterization purposes

were registered. To assess this variation, the on-resistance was monitored in post-analysis (as it is dependent on temperature). As example, one critical measurement point is presented in Fig. 3.12.

From Fig. 3.12, it can be observed that the resistance does increase during high current operation. Following the guidelines of [18], a perfect square pulse generates a juntion temperature rise following the expression

$$\Delta T_J = P * Z_{th}(T_{pulse}) \tag{3.3}$$

in which P is the power of the pulse and Z_{th} is the transient thermal impedance evaluated at the duration of said pulse. However, the pulse in this case is not perfectly squared, and therefore to assess the temperature rise at every point, a simulation using the thermal impedance model of the device has been performed. First of all, please note that the dynamics for the SiC devices are on the hundreds of nanoseconds, and hence changes at the milisecond range are very slow from the device perspective and can be essentially considered steady state with a drift for practical measurement purposes. In other words, it is possible to get any point of the current curve and use the corresponding voltage for forward characterization purposes. This then becomes a trade-off, as selecting points obtained with longer times (for example, 3 ms) present higher temperature rise results by both higher transient thermal impedance and also higher resistance as a consequence of higher temperature. On the other hand, using points selected at the beginning of the pulse (1 ms) presents lower temperature rise, but provide, for example, a 171 A measurement for a 250 A pulse reference, limiting the range of currents from which information can be extracted. Higher reference currents can be set to obtain higher currents at 1 ms, but the device can withstand a maximum of 500 A during 1 ms at 60°C, and therefore there is not much room left to increase reference currents safely.

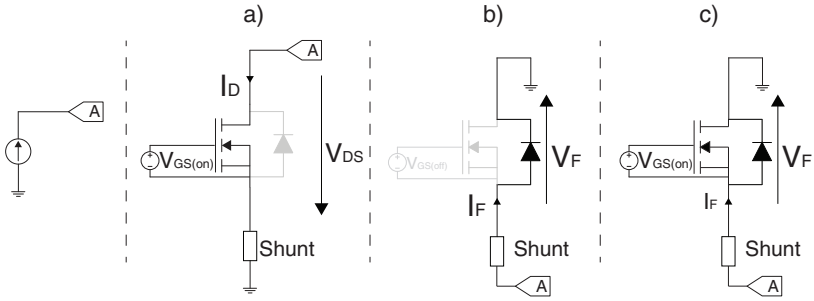


Figure 3.11: On-state module connection Schematic. a) Measurement scheme for the SiC-MOSFET. b) Measurement scheme for the Schottky diode. c) Measurement scheme for the Schottky diode operating in parallel with the SiC-MOSFET channel.

From here, several approaches were evaluated, but ultimately it was decided that all results in the 2 ms range were to be kept to perform the forward measurement curves. This was done so because 2 ms presents a good trade-off between current and device heating. This will of course produce uneven error among measurements, being low current, low temperature measurements more precise. However, simulation results show that at 2 ms, 250 A reference current and T_{J_0} = 125°C present temperature rises of 17°C and 19°C for the MOSFET and diode respectively, which would be a worst case scenario for temperature rise. Reference currents of 200 A for the same conditions already present temperature rises of 12°C and 14°C for MOSFET and diode respectively, which proves that as soon as current is reduced below 200 A, temperature rises are fairly reduced due to the quadratic effect current plays on loss. It is worth noting that this effect is further reduced while using both devices at the same time, as the peak current will be shared between channel and diode and therefore individual conduction loss gets drastically reduced.

These errors however, were deemed acceptable for the objectives of this measurement, as considering these values at T_j = 125°C provides higher voltage drops than what the real value would provide, being a natural worst case scenario event. Additionally, according to datasheet values of $R_{DS(on)}$ resistances, this temperature difference accounts for an approximate $R_{DS(on)}$ resistance difference of 0.8 mΩ, which would mean a 0.2 V voltage difference for a 250 A forward current. This current difference was deemed small enough for the stated objectives of this characterization.

3.2.4 The Gate Unit

The gate unit concept is developed according to the gate driving requirements of the device to achieve its advertised characteristics. Hence, the basic requirements the gate driver needs to fulfill are the following:

- Turn-on voltage $V_{G(on)}$: The gate unit needs to provide stable voltage equivalent to the recommended datasheet turn-on voltage. In this particular case

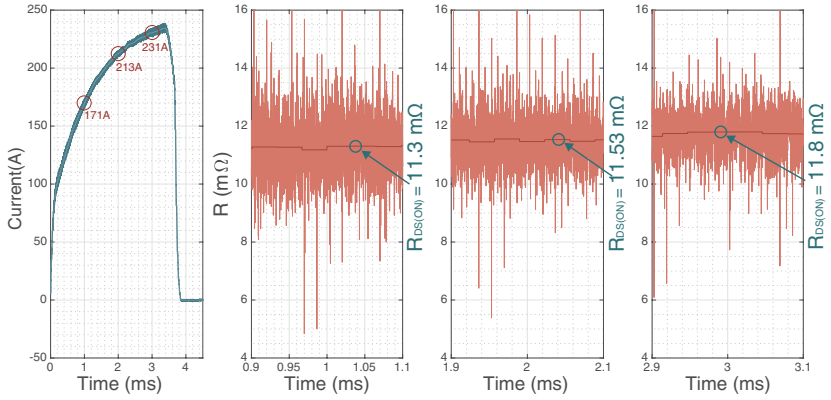


Figure 3.12: SiC MOSFET current pulse example using a 250 A reference current pulse at T_{J_0} = 125°C with R_{DS} analysis at three time windows of 0.2 ms centered on 1, 2 and 3 ms.

the voltage is $V_{G(on)}$ = 18 V.

- Turn-off voltage $V_{G(off)}$: The gate unit needs to provide stable voltage equivalent to the recommended datasheet turn-off voltage. In this particular case the voltage is $V_{G(off)}$ = –2 V.
- Gate current: The gate unit needs to provide enough current to not bottleneck the device nominal switching speed. The maximum required peak current will occur when switching states through the smallest gate resistance, as this will trigger the highest current flow. In the case of this module, this occurs during turn-off, as the turn-off resistance and the internal gate resistance represent the lowest gate resistive path during switching transients. This current is calculated as:

$$I_{G(peak)} = \frac{V_{GS(on)} - V_{G(off)}}{R_{G(off)} + R_{G(int)}} = \frac{18 - {}^{-}2\,V}{0.2 + 1.8\,\Omega} = 10\,A \tag{3.4}$$

- Gate driver power: The power supply of the gate unit needs to provide more output power than the estimated gate driver loss at operating frequency. In this particular case, since the gate charge Q_G is known and needs to be taken in and out of the gate source capacitor at a frequency equal to the switching frequency, the average current can be approximated as $Q_G f_{sw}$. Since this charge needs to be moved periodically in and out with a $\Delta V_G = V_{G(on)} - V_{G(off)}$ voltage gradient, the average gate unit loss can be calculated as expressed in:

$$P = \Delta V_G f_{sw} Q_G = 0.68\,W \tag{3.5}$$

and in this case, since the converter switching frequency is f_{sw} = 20 kHz, the estimated loss per gate is 680 mW.

- Low inductive paths: The gate unit must have short, low inductive paths to the gate and kelvin source in order to avoid voltage peaks, oscillations, and a slower current rise.
- Isolation: The gate unit must provide enough isolation between control signals and power stage signals to ensure safe operation. Hence the isolation capability of the gate unit needs to be at least capable of isolating the planned DC-Link voltage plus the maximum possible voltage overshoot and a sufficient safety margin. In this particular case, isolation was designed according to the 1.7 kV blocking voltage of the devices, and also considered as requirement DC/DC converters with low coupling capacitance, so common mode currents due to the switching transients of power signals observed a high impedance path to cross the isolation barrier.

Additionally, the gate unit can feature additional characteristics that provide extended functionality and prevent/mitigate unexpected/faulty behavior. Some of these characteristics are:

- Crosstalk attenuation

  Because of the parasitic capacitance C_{GD}, when turning-on one switch of the halfbridge, the dv/dt over the complimentary MOSFET capacitance C_{GD} can potentially generate a current flowing into the gate and turn the device on, generating a short on the leg for a small amount of time. In the case of SiC-MOSFETs, since they still present non negligible resistance right after the gate voltage crosses the threshold voltage, the effect does not generate a hard short, but it does produce increased losses. In case this effect is present, some strategies to mitigate this effect can be introduced at the gate unit level, such as reducing the turn-off resistor value in the blocking state, implement active miller clamping [76], put a capacitor in parallel with the C_{GS} capacitor, or use more elaborate schemes such as using resonant circuits on the gate [77], use higher than recommended gate driving voltages temporary during the potential crosstalk time window [77], or creating additional current paths [78], among others.
- Overvoltage protection

  Because of parasitic inductances in the circuit, switch devices experience voltage overshoots at turn-off while the current decreases and, if this voltage surpasses the rated blocking voltage of the device, it can drive it into avalanche mode. To protect the device, different methods can be implemented. Among them the classic solutions, there is active clamping [79], which consists on using an avalanche rugged diode to clamp the maximum voltage of the switch during the overvoltage event.
- Short circuit detection/protection

  In case of short circuit, it is possible to use the gate unit to detect shortcircuit events. Some strategies are desaturation (DESAT) detection [80], which consists in detecting when the switch goes out of the normal V_{DS} voltage due to the increase in drain current, or $L\sigma$ detection [81], which consists on measuring the voltage over the stray inductance between the source and the kelvin source in order to detect the short circuit event. These methods can, after detection, take additional measures, such as turn-off the device and communicate the fault back to the control unit. Additionally, because of high currents due to the short circuit event, soft turn-off methods may be

Table 3.5: Gate unit requirements.

Parameter	Value
Turn-on Voltage	18 V
Turn-off Voltage	–2 V
Peak current	10 A
Gate unit power per switch	680 mW
Shortcircuit detection	$< 2\,\mu s$
Shortcircuit protection	Desat detection and Lσ detection
Additional	Soft Turn-off, low inductive paths, symmetric construction, error detection

necessary in order to avoid overvoltages above the rating of the device.

- Error management

  Additionally, the gate driver can feature different error management measures, such as automatic turn-off in case of detecting an anomaly (shortcircuit for example), require a hard-reset in case of failure, communicate with other gate drivers/main control unit to report the failure, etc.

For this project, the ideal gate unit was described with the requirements presented in Table 3.5.

For this project, three gate units were developed, and they are referred to as GUV1, GUV2 and GUV3 respectively. The first gate drive unit (GUV1) is a modified version of a Si-IGBT driver previously developed by the TU-Dresden chair of power electronics for fast switching Si-IGBTs. This gate unit is directly mounted over the SiC-MOSFET module, communicating with the control platform through cable using low voltage differential signaling (LVDS). This version of the gate unit had the main objective of characterizing a single device, while also gathering data and experience in driving and measuring SiC devices to then use this information to develop a second gate unit tailored for these SiC-MOSFET modules. The main modifications over the original IGBT gate unit design were the driving voltages, which are +18 V and -2 V instead of the +18 V and -9 V the gate unit originally produced. Additional modifications were necessary such as the deactivation of Si-IGBT designed security measures, and a small circuit to trick the ACPL-339j so it would not go into undervoltage lockout with -2 V negative voltage. These modifications were carefully performed to minimize the length of the additional paths, while soldering components directly to each other to minimize current paths. The GU performed well with over 7 resistance pairs, providing crucial data for the development of the second gate unit (GUV2). Both the 3D version of the gate driver unit and its implementation are presented in Fig. 3.13.

The second version of the gate (GUV2) was constructed considering the obtained data from the experiments performed with the first version. It is especially designed to drive parallel-connected SiC modules and it features symmetric construction, better DC/DC converters with smaller coupling capacitances and higher isolation capability, communications through cable and/or optical interface, and improved common mode paths. Additionally, two short circuit detection methods (Lσ and Desat detection) supported by a CPLD for timing and error communication were implemented, but its usage is part of another dissertation of the TU-Dresden chair of power electronics. The whole design considers

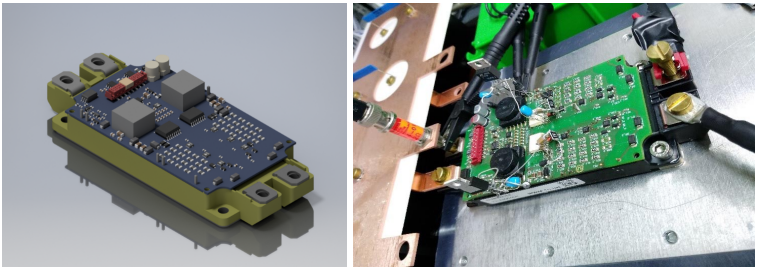


Figure 3.13: First version of the gate unit (GUV1) based on the fast Si-IGBT gate driver. Left: 3D model of the gate driver. Right: Implementation of the modified gate unit.

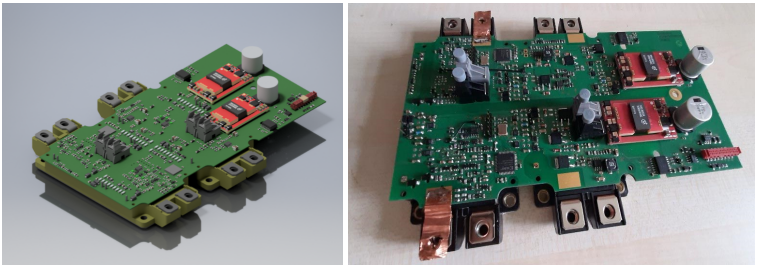


Figure 3.14: Second version of the gate unit (GUV2) for parallel connection of SiC Devices. Left: 3D model of the gate. Right: Implementation of the gate unit.

a direct connection between module sources to enforce simultaneous switching of the parallel-connected modules. Both the 3D version of the gate unit and its implementation are presented in Fig. 3.14.

Finally, the third version of the gate unit (GUV3) was developed. It is fundamentally a redesign of the GUV2 into a smaller form factor to fit the layout of the converter prototype, which required a stacked PCB design. The top board receives the signals and provides power to the GU through the isolated DC/DC converters, while the lower board feature the power stage of the gate unit in charge of powering the gates of the corresponding switches. Two important modifications since the previous version were performed, and these are the inclusion of sockets in the gate unit in order to include a short circuit detection method in post as a modular solution, and the second change is the inclusion of 0.2 Ω in the source paths, to limit the current flowing through the kelvin sources, fact that has been measured and confirmed to be in safe margins. Both the 3D version of the gate unit and its implementation are presented in Fig. 3.15.

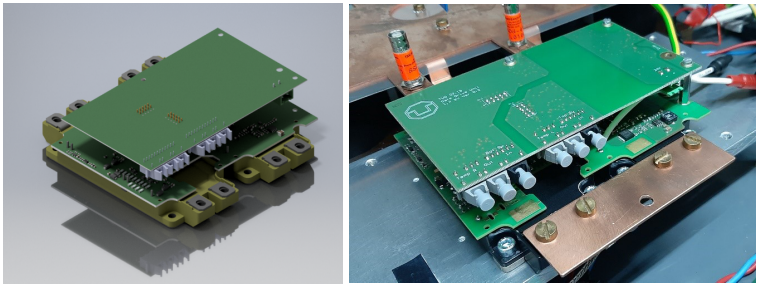


Figure 3.15: Third version of the gate unit (GUV3) for converter prototype construction. Left: 3D model of the gate unit. Right: Implementation of the gate unit.

Table 3.6: Summary of parameters on the performed DPT experiments

Parameter	Tested values
V_{DS}	{ 900, 1000, 1100 } V
I_D	{ 25, 50, 75, 100, 125, 150, 175, 200, 225, 250 } A
T_j	{ 25, 125 } °C
$R_{G(on)}$	{ 0.789, 1.6, 2.5, 3.3, 5.5, 6.6, 8.25 } Ω
$R_{G(off)}$	{ 0.58, 1.175, 3.3, 5.5 } Ω

3.2.5 Experimental Investigation of the Behavior of the SiC-MOSFET Module

The characterization of the SiC-MOSFET module as a standalone device was performed using the first version of the gate unit (GUV1). In the following sections, the parameters of the experiment rows and main measurement results are presented, followed by a discussion of the obtained data.

Switching Transient Results

The transient characterization of the SiC device has been performed by changing gate resistors and subsequently performing measurements at 900 V, 1000 V, and 1100 V, from currents ranging from 25 to 250 A at 25 A intervals, both at 25 and 125°C. These double pulse test events were then analyzed and both timing data and energy loss were also registered. A summary of the performed experiments is presented in Table 3.6

To summarize, the main objectives of the DPT measurements are to determine:

- MOSFET turn-on transient: signals vs time, timing data, dv/dt, di/dt, and switching energy loss.
- MOSFET turn-off transient: signals vs time, timing data, dv/dt, di/dt, and switching energy loss.

- Diode turn-off transient: signals vs time, timing data, dv/dt, di/dt, and reverse recovery loss.

In the case of single module measurements, the turn-off and turn-on pulses lasted 20 µs each, ending the experiment at the 40 µs mark. Hence, the turn-off event was captured at t_{off} = 0s and the turn-on event at t_{on} = 20 µs respectively.

For sake of brevity, and to avoid drowning the reader in figures for every parameter, only the most relevant data considering discussion purposes and their corresponding impact in design is presented.

1. Transient Signals in Time

In Figs. 3.16 and 3.17, the transient signals v/s time of both the SiC-MOSFET and SiC-diode turn-off event are presented respectively. These signals are presented at a blocking voltage of 1100 V, max. measured current, and a junction temperature of T_J = 125°C as these values are closer to operating conditions than T_J = 25°C and are therefore more relevant to the discussion. All signals are delay corrected in order to be graphically comparable. Additionally, three representative gate voltage measurements for the same conditions are presented in Fig. 3.18.

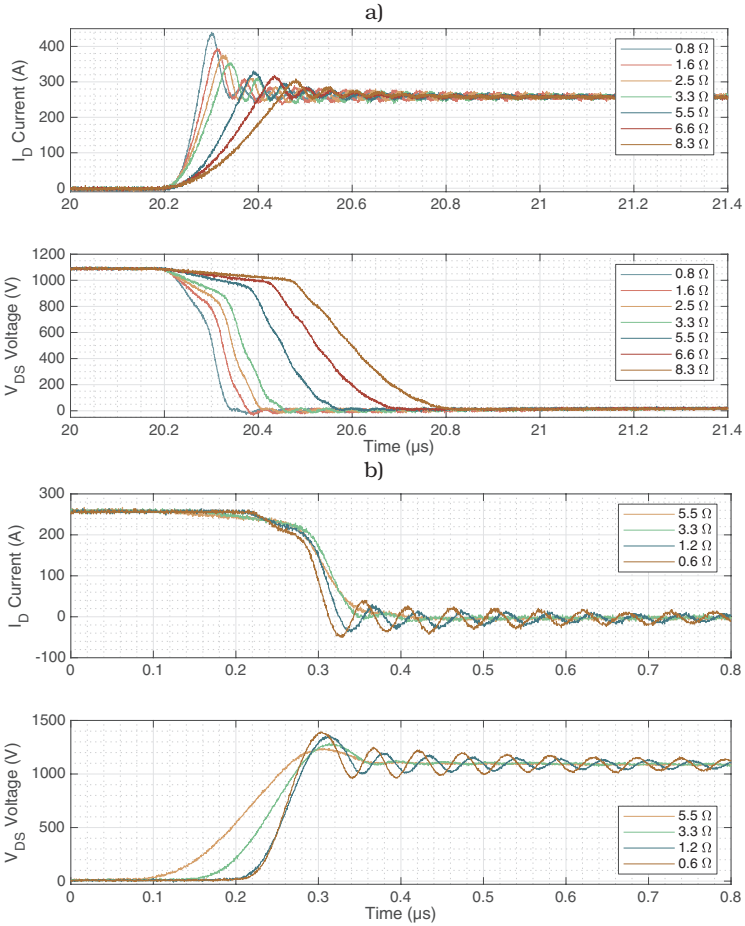


Figure 3.16: Delay corrected SiC-MOSFET transient signals for I_D = 250 A, V_{DS} = 1100 V and T_J = 125°C. a) I_D and V_{DS} during the turn-on transient for all measured turn-on gate resistances. b) I_D and V_{DS} during the turn-off transient for all measured turn-off gate resistances.

Regarding MOSFET turn-on transient signals Fig. 3.16, turn-on currents can achieve significant overshoot as a result of peak reverse recovery currents. The maximum current overshoot registered in all experiment rows was captured with $R_{G(on)}$ = 0.8 Ω, reaching a peak current of 440 A. This current is a 76% higher than the nominal current of the module, but well within the maximum pulsed current of the device (500 A for less than 1 ms), which is also a reassuring indicator when considering that the datasheet recommended $R_{G(on)}$ = 1 Ω. Current rise times t_{ri} range from 166 to 40 ns for the biggest and smallest turn-on gate resistances respectively. On the other hand, no noticeable oscillations can be observed in V_{DS}, presenting a voltage drop during current rise as a result of the parasitic inductance. In contrast with Si-IGBTs, the drop in this case is not constant, as a consequence of variable di/dt during the turn-on event. Voltage fall times t_{fv} range from 245 to 94 ns respectively.

On the other hand, referring to the turn-off transient signals in Fig. 3.16, both current and voltage transitions result in oscillations after the switching event. This is due to the fact that while turning off, the MOSFET builds a depletion layer, hence decreasing its output capacitance C_{oss}. This enables the possibility of resonances between the total stray inductance of the circuit and this capacitance. In this case, and using datasheet based data of the C_{oss} capacitance while blocking voltage, the calculated resonant frequency is approximately 20 MHz, which matches what can be observed in the figure. It should be noted though, that there are gate resistance values that can damp oscillations altogether, avoiding the excitation of this resonant mode while still providing relative fast turn-off transients. Current fall times t_{fi} range from 97 to 70 ns, while the voltage rise time ranges from 116 to 44 ns. It is also interesting to note that datasheet provided information typically only mention current rise and fall times, referring to these magnitudes as rise or fall time alone, which only provides half of the picture, as it can be observed here.

When observing the diode turn-off characteristics, (see Fig. 3.17), the same oscillation that was previously observed at turn-off is observed here due to the same factors. The C_{oss} of the device blocking voltage at the moment presents a depletion layer and hence the same capacitance values presented in the turn-off event. This results in producing the same resonant frequency. However, the oscillations can in this case occur during the voltage transition, increasing the overall dv/dt. The diode is accountable for the highest dv/dt values in the circuit, and therefore should be the first observed magnitude when suspecting crosstalk, common mode transient immunity issues, or optocoupler signal errors in the system.

Gate voltage measurements are presented in Fig. 3.18. These voltages were performed using passive probes, as these demonstrated the best dynamic characteristics for this measurement. However, since voltages of the kelvin source pin referred to ground during transients could present oscillations of over 100 V, 20-50 V per division scales had to be used when measuring high current. This negatively impacted resolution, and signals had to be additionally filtered in order to be usable for timing purposes. When observing turn-on gate voltages, while using the biggest resistance the miller plateau is clearly visible, taking almost 150 ns to reach steady state. On the other hand, while increasing speed, the gate stray inductance produces a resonant circuit with the gate capacitance leading to a peak and a subsequent resonance in the measured gate voltage, as it can be seen in the results of the other two $R_{G(on)}$ resistances. At turn-off, the

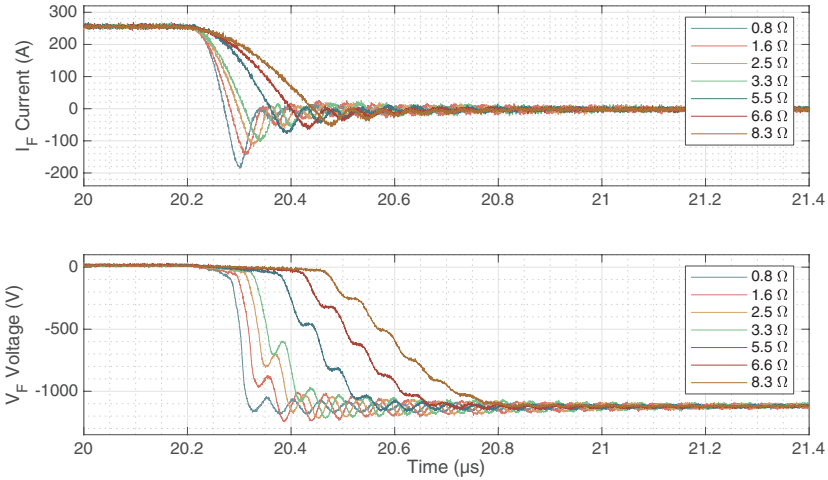


Figure 3.17: Delay corrected SiC-Diode turn-off transient I_F and V_F signals for I_F = 250 A, V_F = 1100 V and T_J = 125°C for all measured turn-on gate resistances.

same behavior can be observed, the gate voltages drop to the miller plateau, and then further until crossing the threshold voltage, to finally settle at the turn-off voltage. The problem of this measurement is however, that the kelvin source voltage oscillates with high voltage magnitudes during the transient, making the extraction of usable differential measurement of the passive probes challenging, as any extra inductance observed by one passive probe will not be compensated by the other while performing the difference, which will generate undamped oscillations as observed in the figure. This effect forbade the measurements of the upper MOSFET gate voltages, in which this effect is more severe. For this reason, crosstalk risk and behavior had to be assessed indirectly by observing current and voltage signal shape variations, along switching loss data.

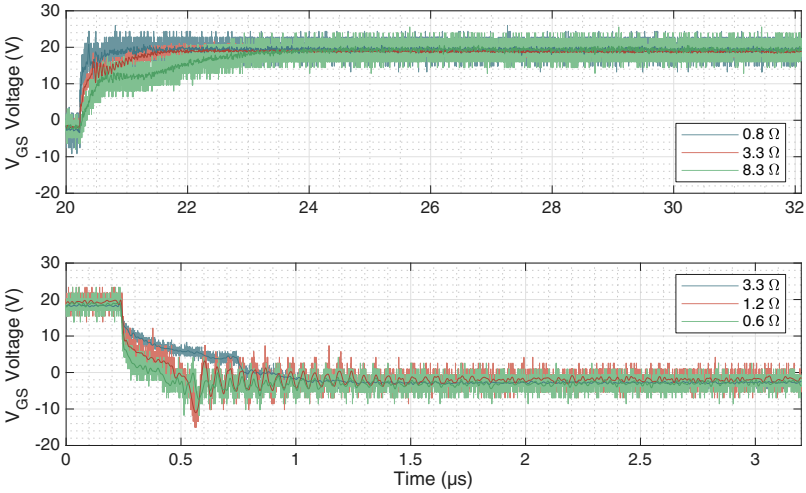


Figure 3.18: Delay corrected SiC-MOSFET gate voltage signal V_{GS} for I_F = 250 A, V_F = 1100 V, T_J = 125°C and three representative resistance pairs. Up: Turn-on transient. Down: Turn-off transient.

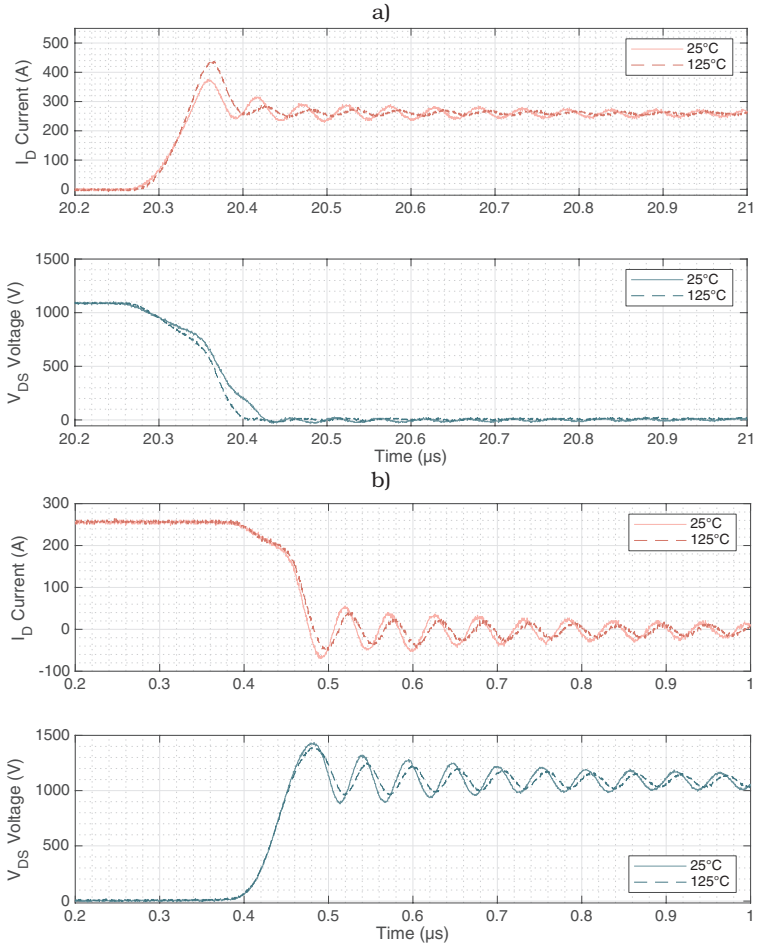


Figure 3.19: Delay corrected SiC-MOSFET transient temperature dependency for I_D = 250 A, V_{DS} = 1100 V. a) MOSFET turn-on transient with $R_{G(on)}$ = 0.8 Ω. b) MOSFET turn-off transient with $R_{G(off)}$ = 0.6 Ω.

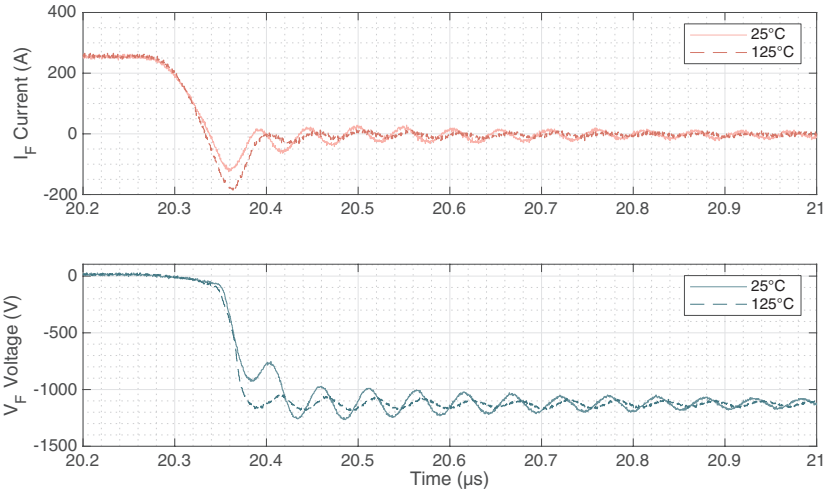


Figure 3.20: Delay corrected SiC-Diode turn-off transient temperature dependency for I_D = 250 A, V_{DS} = 1100 V and $R_{G(on)}$ = 0.8 Ω.

Finally, the transient behavior temperature dependency of the MOSFET and diode signals is presented in Figs. 3.19 and 3.20 respectively. As it can be observed in the MOSFET turn-on, although the device presents higher peak current due to higher diode reverse recovery current with increased temperature, the voltage falltime is decreased, and hence the effect on loss should balance or decrease. On the other hand, turn-off behavior is quite resilient to temperature, and only a slightly slower current falltime is observed, impacting also the magnitude of the turn-off current and voltage oscillations. Finally, diode transient behavior is the most affected by temperature, as both a higher reverse recovery current and a higher diode dv/dt is observed.

2. MOSFET and Diode di/dt

   MOSFET and diode di/dt characteristics are useful to determine voltage variations due to parasitic stray inductances during transient events. However, since the lower MOSFET and the upper diode share current shape during MOSFET switching events, their di/dt values are the same, and therefore only MOSFET values will be discussed. After observing the different MOSFET di/dt current results, it was concluded that the highest values are observed at 25°C for the MOSFET turn-off event, and 125°C for the MOSFET turn-on event; and the results are shown in Fig. 3.21.

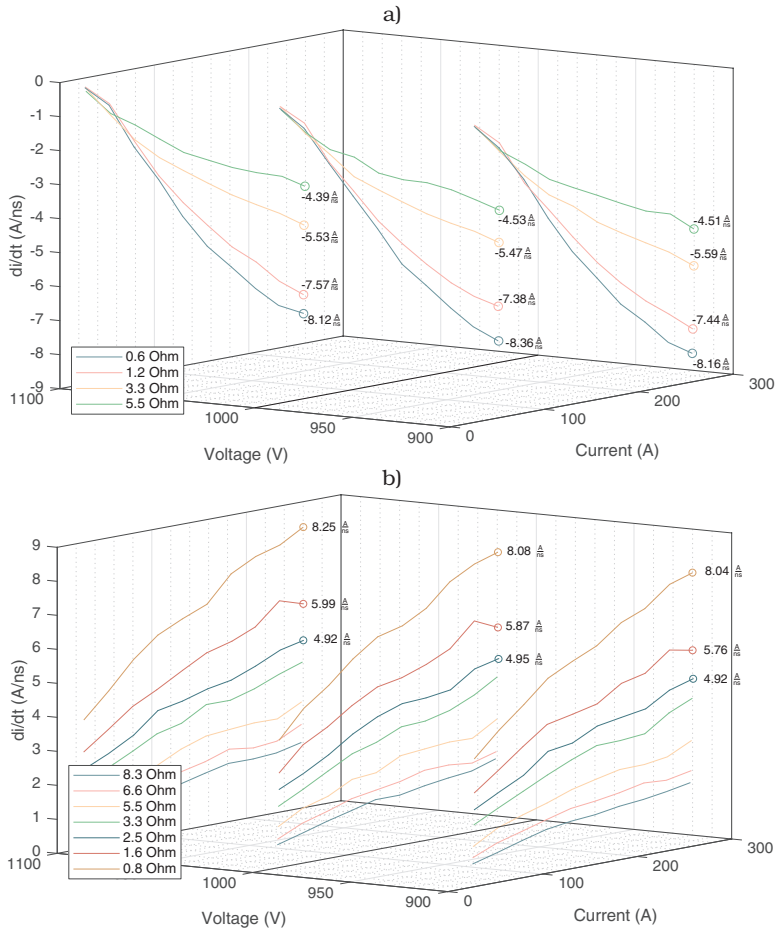


Figure 3.21: Critical di/dt values for the SiC-MOSFET/Diode transients. a) MOSFET di/dt turn-off transient values at 25°C. b) MOSFET di/dt turn-on transient values at 125°C.

As an interesting remark, since turn-off events generate V_{DS} overvoltage peaks during the event, their critical scenario happens at room temperature and not at 125°C. Observing Fig. 3.21, during turn-off, the worst case scenarios for turn-off di/dt happen while using the smallest resistance, resulting in a total maximum of 8.12 A/ns, which considering the observed app. 40 nH of stray inductance (from the device standpoint), matches voltage overshoots of close to 1400 V during turn-off at room temperature. This voltage overshoot is not such a critical issue for SiC-MOSFETs as it is for Si-IGBTs, as the avalanche voltage of this device has been confirmed by manufacturer to be above 2 kV. On the other hand, regarding lifetime, the 100 FIT of these SiC-MOSFET devices is close to 1700V instead of the 1350V that typical Si-IGBTs in this same voltage class feature (an example of this effect can be seen in [35] for 1200V devices). Meanwhile, during turn-on, the maximum observed di/dt values are similar, being the critical one 8.25 A/ns, however, this value only decrease the voltage drop on the MOSFET during the transient, and are therefore not critical. Additionally, it should be noted that this effect does not present a dependency on blocking voltage, which is to be expected as current variation during the transition is only determined by the device transconductance when the gate voltage is between the Miller plateau and the MOSFET threshold voltage.

3. MOSFET and Diode dv/dt

   Analysis of dv/dt values during transients can be crucial to ensure correct operation of the device, as there are several undesired effects associated with dv/dt, such as Miller currents, MOSFET failure mechanisms and common mode currents among others. Among all processed values, the worst case of MOSFET turn-on dv/dt was at 125°C and I_D = 25 A, where it reached 25 V/ns with the smallest tested gate resistance. However, it presents a slight linear decrease as a function of I_D. On the other hand, MOSFET turn-off dv/dt worst case scenario presents itself at 25°C and I_D = 250 A, reaching almost 25 V/ns as well.

   However, the critical case scenario presents itself at diode turn-off. As it can be observed in Fig. 3.22, critical diode dv/dt values occur at 125°C and 250 A, and can generate during diode turn-off up to 53 V/ns. High dv/dt could potentially generate a parasitic turn-on event in the MOSFET device that is in parallel to the diode through Miller current, and therefore careful observation in energy and switching signals for this point are to be considered if its gate voltage is not being measured. Additionally, this dv/dt could potentially turn on the parasitic NPN transistor of the MOSFET parallel to the diode. Regarding this data, ROHM declares in [35] that failure mechanisms for both their MOSFETs and diodes have not been observed operating with dv/dt up to 50 V/ns. Therefore, gate resistances slightly higher than 0.8 Ω would be recommended. Because of this, and since the manufacturer recommends 1 Ω as $R_{G(on)}$, no smaller gate resistances than this have been used in parallel connection. Additionally, since devices typically have to be de-rated in parallel connection to ensure reliable operation, additional margin from these high dv/dt events should be obtained.

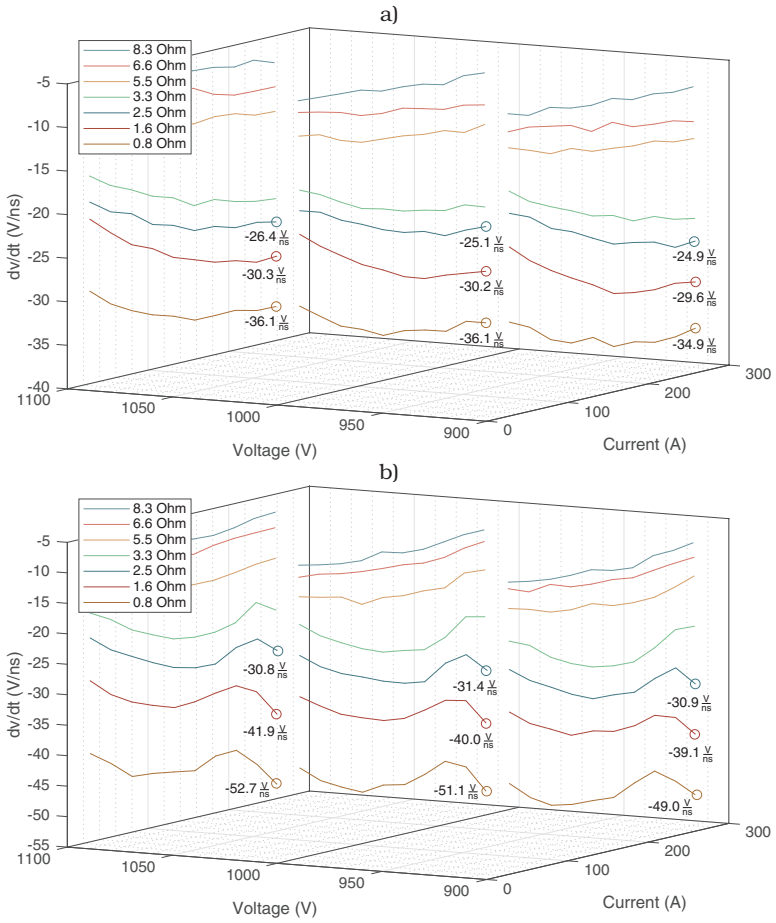


Figure 3.22: Critical dv/dt values for the SiC-Module: Diode turn-off dv/dt transient values. a) Results at 25°C. b) Results at 125°C.

4. Timing Data

Additionally, timing data for all switching events have been captured in order to evaluate device transient speeds depending on driving resistances. To that end, two table summaries for both turn-off and turn-on for the slowest and the fastest tested gate resistance pairs can be found in Table 3.7. It is important to consider that turn-on/off delay is defined in this work (as seen in Fig. 3.4), from the gate voltage 10% change to the current first 10% change, and therefore when considering total switching time, a good approximation for turn-on time is $t_{on} = t_{d(on)} + t_{ri} + t_{fv}$, in contrast with turn-off time $t_{off} = t_{d(off)} + t_{fi}$.

Table 3.7: Timing values for the highest and lowest gate resistance pairs of all tests. Values in nanoseconds (ns).

		$R_{G(on)} = 8.25\,\Omega$, $R_{G(off)} = 5.5\,\Omega$				$R_{G(on)} = 0.79\,\Omega$, $R_{G(off)} = 0.58\,\Omega$			
		25°C		125°C		25°C		125°C	
		25 A	250 A	25 A	250 A	25 A	250 A	25 A	250 A
900 V *ON*	t_{ri}	74	210	59	169	16	47	14	40
	t_{fv}	186	296	148	219	63	118	51	90
	t_{don}	174	253	143	204	54	70	47	63
	t_{on}	537	905	570	948	149	204	124	162
900 V *OFF*	t_{fi}	219	82	238	98	163	57	165	62
	t_{rv}	166	98	178	103	112	39	111	39
	t_{doff}	763	615	763	615	262	201	262	201
	t_{off}	982	697	1001	713	425	258	427	263
1100 V *ON*	t_{ri}	73	206	58	167	16	47	15	40
	t_{fv}	212	332	170	246	66	119	55	94
	t_{don}	166	243	137	198	53	71	47	62
	t_{on}	432	700	460	733	156	211	133	176
1100 V *OFF*	t_{fi}	250	85	272	97	185	65	186	70
	t_{rv}	184	110	198	116	127	43	128	44
	t_{doff}	760	636	760	636	260	203	260	203
	t_{off}	1010	721	1032	733	445	268	446	273

From the table, several interesting assertions can be made such as:

- Using the values of Table 3.7 (smallest resistance pairs in test), the device maximum turn-on time will occur at 25°C and V_{DS} = 1100 V and I_D = 250 A, taking 211 ns. Meanwhile, the maximum turn-off time will also occur at 1100 V but at I_D = 25 A, being temperature independent for practical purposes, and takes 446 ns. These should be the times to consider to set dead-time values for control purposes when using this resistance pair.
- Considering the values of Table 3.7, (the smallest resistance pair in test), the overall slowest switching combination for the same temperature and current is T = 25°C, V_{DS} = 1100 V and I_D = 25 A, and therefore a first ap-

proximation of the theoretical maximum in the most ideal conditions for this device switching frequency would be f_s = 1.664 MHz and dutycycle 26%, or 1.124 MHz and dutycycle 50%, being the turn-off process the limiting timing factor. This is of course a very idealized estimation, as switching loss alone should limit the frequency below 100 kHz [16].

- Referring to Table 3.7, it is interesting to observe that a SiC-MOSFET module can be driven slow to extreme extents, taking almost 1 µs for both turn-on and turn-off in different circumstances.
- From both tables, one important observation to extract from here is that datasheet provided rise/fall times should not be used to assess switching speed. Datasheet provided rise/fall times are always referred to current, and as it can be observed here, that is only one component of the switching process, and although it is tempting to use these values to perform a first order assessment of the switching speed, they can be misleading. This is specially important when comparing to Si-IGBTs, as the datasheet rise times may look similar or not too far apart, which could lead to wrong conclusions.

5. Switching Energy Loss

One of the most important parts of the DPT procedure was to calculate the overall switching loss, as they are direct input to thermal simulations which at the end define the theoretical nominal current. To that end, MOSFET turn-on switching loss, turn-off switching loss, and diode reverse recovery energy have been measured for 25 and 125°C, and the corresponding results are presented in Figs. 3.23, 3.24, and 3.25 respectively.

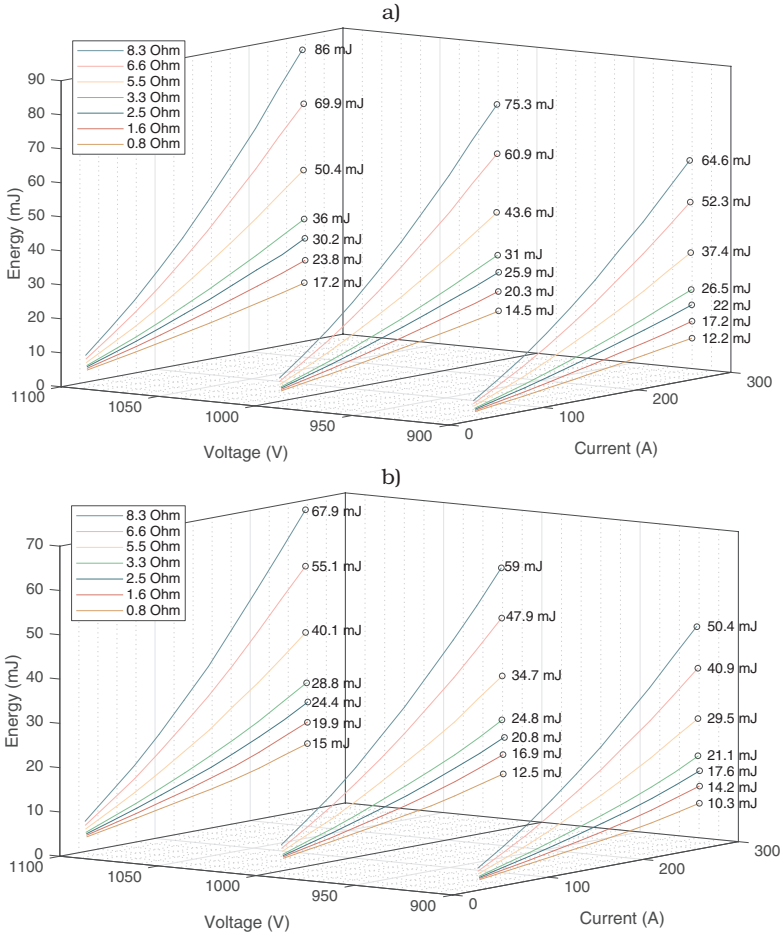


Figure 3.23: MOSFET turn-on energy loss as a function of I_D and V_{DS} for every tested gate turn-on resistance pair. a) Energy loss results for T_J = 25°C. b) Energy loss results for T_J = 125°C.

In Fig. 3.23, it can be observed that the device reduces overall turn-on switching loss when raising temperature, being able to turn-on the module nominal DC current at 1100 V for as little as 15 mJ for V_{DS} = 1100 V and T_J = 125°C. However, $R_{G(on)}$ could be risen as a trade-off for lower dv/dt, without generating excessive additional loss. Further analysis from turn-on loss among 900, 1000 and 1100 V shows energy differences ranging from a [min max] of [14 19]% among 900 and 1000 V results, and a [15 20]% difference between 1000 and 1100 V results (for 125°C). Strictly referring to the averages, for the corresponding ranges these are 16.1 and 17.3% respectively, which is useful for modeling purposes.

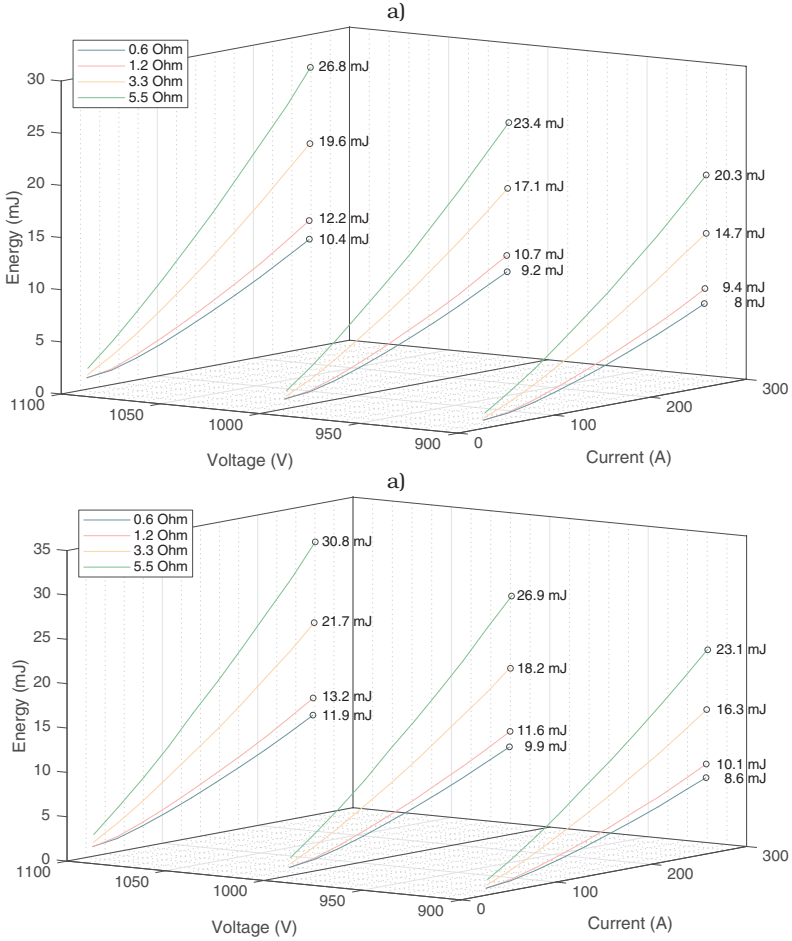


Figure 3.24: MOSFET turn-off energy loss as a function of I_D and V_{DS} for every tested gate turn-off resistance pair. Left: Energy loss results for T_J = 25°C, Right: Energy loss results for T_J = 125°C.

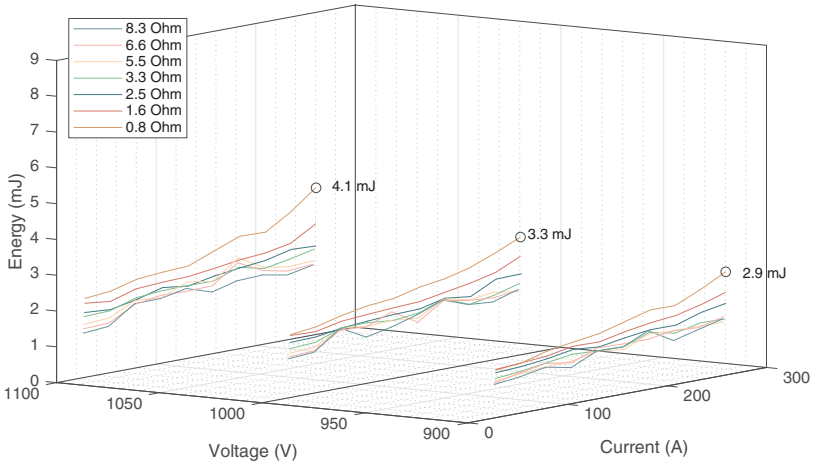


Figure 3.25: Diode reverse recovery loss as a function of I_F and V_F for every tested gate turn-on resistance pair at the critical case scenario: T_J = 125°C.

On the other hand, in Fig. 3.24, it can be observed that the device increases overall turn-off switching loss only slightly when rising temperature, turning the module nominal DC current off at 1100 V for 11.9 mJ in close to operating conditions (V_{DS} = 1100 V and T_J = 125°C). Furthermore, doubling the smallest $R_{G(off)}$ does not increase loss significantly. This is probably because the module internal gate resistance is 1.8 Ω, and therefore the added difference ($R_{G(off)}$ + $R_{G(int)}$) of the two does not substantially change. The same voltage analysis has been performed for turn-off loss among 900, 1000 and 1100 V, and it shows energy differences of [12 23]% among 900 and 1000 V results, and [13 27]% differences between 1000 and 1100 V results (for 125°C). However, the corresponding average error for these ranges is 15 and 16.1% respectively, and furthermore, the biggest differences are observed at low currents, and hence the average values are useful for differences closer to the nominal current.

Finally, only the 125°C case (worst case scenario) for reverse recovery loss is shown, because as it can be seen in Fig. 3.25, these energies are relatively small when compared to switch losses, ranging in the [1 3] mJ range with the sole exception of the $R_{G(on)}$ = 0.8 Ω gate resistance results. In this case, a small increase of the reverse recovery loss as a function of current is observed. However, considering absolute values, the increase is still marginal when compared to MOSFET switching losses. Some possible explanations for this behavior were increased dv/dt, which would act over the junction capacitance of the diode and therefore generate increased reverse recovery current. Another possible explanation could be a soft parasitic turn-on event, as this could generate additional current flow. However, no unexpected behavior has been observed in measured current/voltage signal shapes, or MOSFET switching energy loss to sustain this theory. Finally, it could also be possible that the device is suffering from a small minor-

ity carrier recombination due to the parasitic PiN diode that every SiC Schottky in this voltage range has. As mentioned in the state of art, a P-guard ring must be there to protect the metal semiconductor interface, and reverse recovery energy due to recombination is temperature dependent, which could also be a valid theory for the reverse recovery current increase, and why the corresponding loss increase starts after a certain current value. However, in any scenario the increase is very small, and its value is dwarfed by MOSFET loss. Furthermore, the converter prototype is built with parallel devices, and therefore the nominal current of the modules is unlikely to be reached. For all these reasons, and the high expense to accurately measure the gate voltage of the upper device, this point has been left to be analyzed in the future, as it did not substantially influence converter design.

6. Summary of interesting working points

   To achieve a fast overview of the main consequences of gate resistance selection in resulting switching parameters, two gate resistance pairs designs have been proposed and their results are shown in Fig. 3.26, along with interesting data parameters, which are provided in Tables 3.8 and 3.9 respectively.

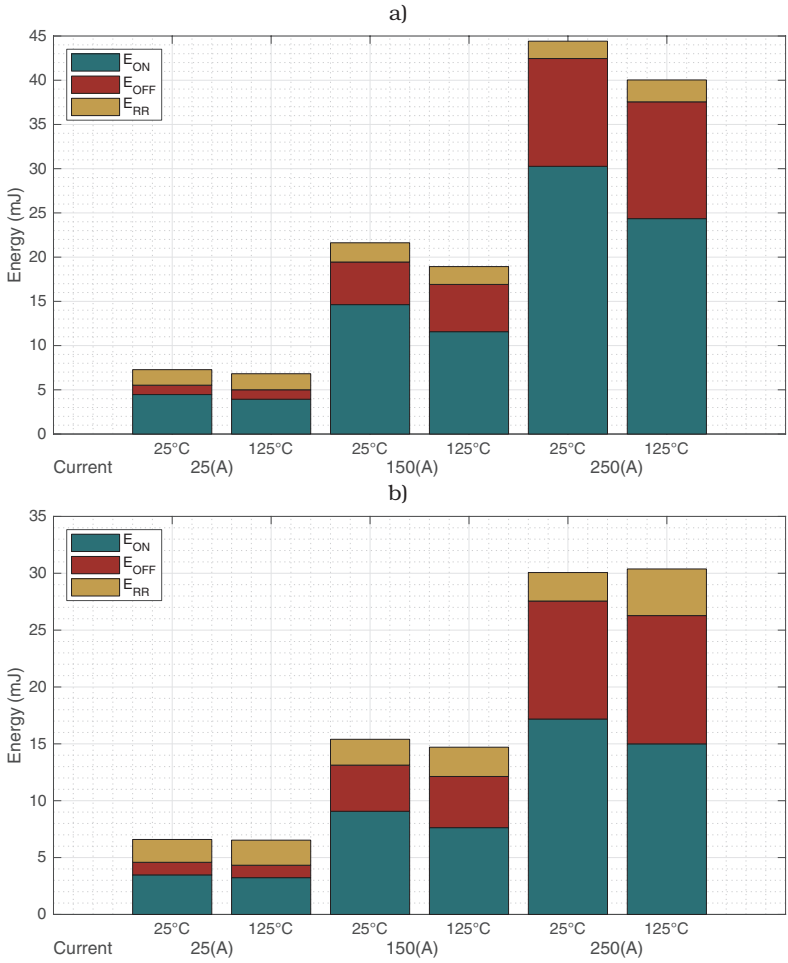


Figure 3.26: Summary of energy loss for different gate resistance pairs for V_{DS} = 1100 V. a) Conservative design: $R_{G(on)}$ = 2.5 Ω and $R_{G(off)}$ = 1.2 Ω, associated data in Table 3.8. b) Fastest design of tested gate resistances: $R_{G(on)}$ = 0.8 Ω and $R_{G(off)}$ = 0.6 Ω, associated data in Table 3.9.

Table 3.8: Conservative design parameters

Param.	1000 V	1100 V
	[ON OFF]	[ON OFF]
$\hat{I_D}$	370 A	376 A
$\hat{V_{DS}}$	1302 V	1391 V
MOSFET $\frac{dv}{dt}$	[17.1 20.3] $\frac{V}{ns}$	[17.1 20.8] $\frac{V}{ns}$
MOSFET $\frac{di}{dt}$	[4.9 7.3] $\frac{A}{ns}$	[5.1 7.6] $\frac{A}{ns}$
Diode $\frac{dv}{dt}$	OFF: 31.4 $\frac{V}{ns}$	OFF: 30.8 $\frac{V}{ns}$

Table 3.9: Fast design parameters

Param.	1000 V	1100 V
	[ON OFF]	[ON OFF]
$\hat{I_D}$	437 A	440 A
$\hat{V_{DS}}$	1340 V	1417 V
MOSFET $\frac{dv}{dt}$	[23.9 24.8] $\frac{V}{ns}$	[25 25.2] $\frac{V}{ns}$
MOSFET $\frac{di}{dt}$	[8.1 8.3] $\frac{A}{ns}$	[8.2 8.1] $\frac{A}{ns}$
Diode $\frac{dv}{dt}$	OFF: 51.1 $\frac{V}{ns}$	OFF: 52.7 $\frac{V}{ns}$

As observed in Fig. 3.26, the SiC module could be switched for less than 30 mJ of switching energy with the smallest pair of tested resistances, at the cost of higher dv/dt, and higher current/voltage overshoots. However, the voltage overshoots are a joined consequence of di/dt and circuit stray inductance, so it must be beared in mind that an actual converter design that does not need to fit the shunt and measurement equipment will have a smaller switching loop stray inductance and thus a smaller voltage overshoot. This is a worst case scenario in that regard. On the other hand, a more conservative design could be built, using bigger gate resistances and in that case the total switching energy can rise up to 45 mJ but reducing dv/dt, and current/Voltage overshoot. It is also interesting to remark, that since in parallel connection the devices will not operate at nominal current, when operated at I_D = 150 A the energy difference between both designs is much smaller, being in worst case almost 6.5 mJ.

On-state Results

The on-state characterization of the SiC device has been performed by changing the driven current through the device and the junction temperature to then measure the resulting drain source/forward voltage. MOSFET, diode and diode with turn-on MOSFET in third quadrant operation have been measured, and the respective experiment parameters are presented in Table 3.10.

However, and as explained in the testbench description, due to the current source testbench dynamics the measurements were not taken when the current source reached steady state, but at the 2 ms mark. Hence the registered currents are smaller than the assigned as setpoints to the testbench.

As it can be observed from Fig. 3.27, the MOSFET fully turn-on presents a linear

Table 3.10: Summary of parameters on the performed on-state experiments.

Parameter	Tested values
I_D	{ 50, 100, 150, 200, 250, 300[1] } A
T_j	{ 25, 60, 90, 125 } °C

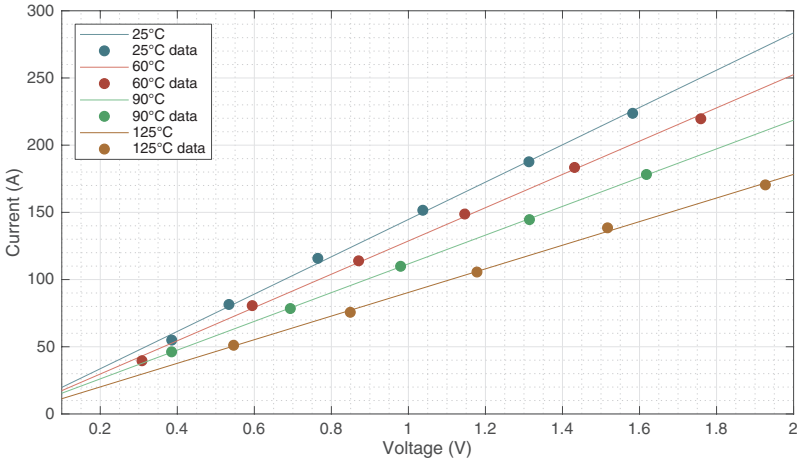


Figure 3.27: MOSFET forward measurements for gate voltage $V_{G(on)}$ = 18V.

dependence between I_D and V_{DS} as expected, since it should only present a resistive behavior according to MOSFET forward equations described in chapter 2. Furthermore, these values are close to datasheet provided data, which is to be expected as this measurement is most of all, temperature dependent, and therefore should not change much from setup to setup.

Following with the diode forward measurement in Fig. 3.28, for all practical purposes, a linear behavior can be observed in the measured range. The absence of exponential curve behavior values can be explained also by the equations in chapter 2. The diode has logarithmic behavior added to a resistive component which is the sum of the drift resistance, contacts, etc. So, as long as the resistive part dominates the voltage drop, the observed characteristic will look linear. Otherwise it will look logarithmic (or exponential if the voltage is in the x axis) until the current is high enough for the resistive part to dominate the voltage drop. This resembles datasheet provided data in the measured range.

Finally, observing Fig. 3.29, the MOSFET fully turn-on with the diode in third quadrant presents an exponential behavior in almost all measured situations, but this is a measurement limitation and it should become linear after the exponential component of the voltage drop ceases to dominate. The reason for this curve shape in this case obeys the same explanation for the diode, when sharing the current among the two devices, the voltage drop on the resistor will

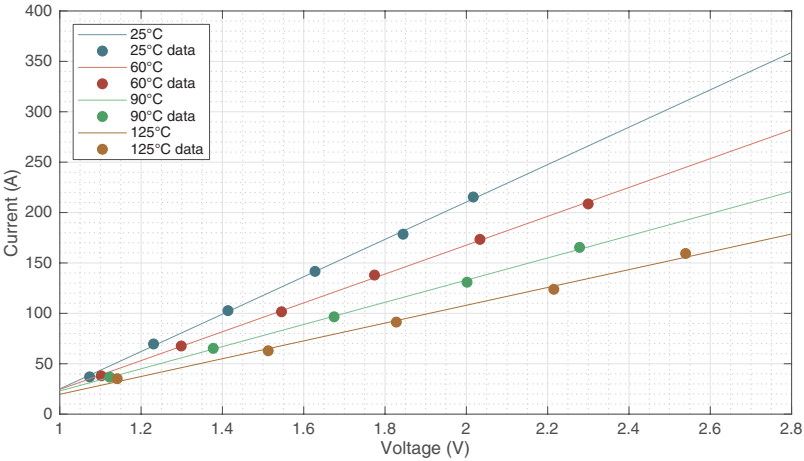


Figure 3.28: Diode forward measurements. MOSFET gate voltage $V_{G(off)}$ = –2V.

determine the voltage drop over the diode, and therefore, since there is less current flowing through the diode and influencing its behavior, the exponential part dominates, shaping the curve as described. This can be observed in the 125°C curve, in which the end of the curve is perfectly fitted by the linear expression, but the beginning of the curve would be better fitted to an exponential behavior.

All measurements are fairly close to datasheet provided results, being the datasheet slightly more conservative in general and with observed differences of less than 10% in the worst cases. However, the available range provided by the measurements is fairly limited and an extrapolation would probably lead to additional error. Hence the datasheet curves have been deemed acceptable for simulation purposes, as they should yield a slightly more conservative design, while also providing data in a wider voltage/current range.

In summary, it has been deemed that datasheet provided data is adequate for modeling device conduction loss.

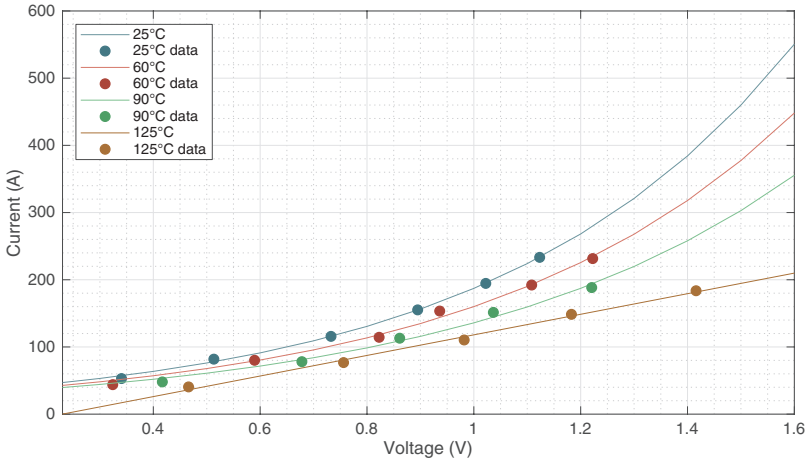


Figure 3.29: Diode and MOSFET channel 3rd quadrant measurements. MOSFET gate voltage $V_{G(on)}$ = 18V.

3.2.6 Comparison of the SiC-MOSFET and an Equivalent Si-IGBT

Along with this study, a comparison against a Si-IGBT was performed, and these results were published in the paper: "Comparison of 1700 V SiC-MOSFET and Si-IGBT Modules Under Identical Test Setup Conditions" [16]. Some remarks and interesting analysis of characteristics and device losses are summarized here but for the complete work the reader is kindly referred to the corresponding publication.

First, the compared devices were the ROHM BSM250D17P2E004 SiC-MOSFET module and the Infineon FF300R17ME4 Si-IGBT module (see Fig. 3.30). The main characteristics that justified their suitability for a fair comparison are presented in Table 3.11, but in simple terms, they presented similar thermal characteristics, while being similarly rated and presenting identical package dimensions. In other words, the comparison was made from an application standpoint (device rating and similar package), instead of a device technology stand point (identical semiconductor area for both technologies).

To that end, the same DPT testbench that was used in this work was operated to perform this comparison. The only changes are gate unit driving values, particularly driving voltage and gate resistances, which were changed to operate the Si-IGBT with manufacturers recommended values.

Waveforms and corresponding energy loss

From the obtained comparison of waveforms and energy loss data, a summary of interesting curves is summarized in the following figures:

Figure 3.30: Compared half-bridge modules. Left: Infineon FF300R17ME4 (Si-IGBT+Si-Diode) [14]. Right: Rohm BSM250D17P2E004 (SiC-Mosfet+SiC-SBD) [15].

Table 3.11: Main characteristics of the compared modules according to datasheet data.

Parameter	BSM250D17P2E004 SiC-MOSFET module	FF300R17ME4 Si-IGBT module
V_{DS}/V_{CE} max	1700 V	1700 V
I_D/I_C	250 A@T_c = 60°C	300 A@T_c = 100°C
R_{thjc}Sw	0.083 °C/W	0.083 °C/W
R_{thjc}Diode	0.114 °C/W	0.130 °C/W
Configuration	Half-bridge	
Package	EconoDUAL package	
Maximum dissipation	1800 W	1800 W
High qty. order cost (as of 25.06.2020)	618 $ USD per unit.	126 $ USD per unit.

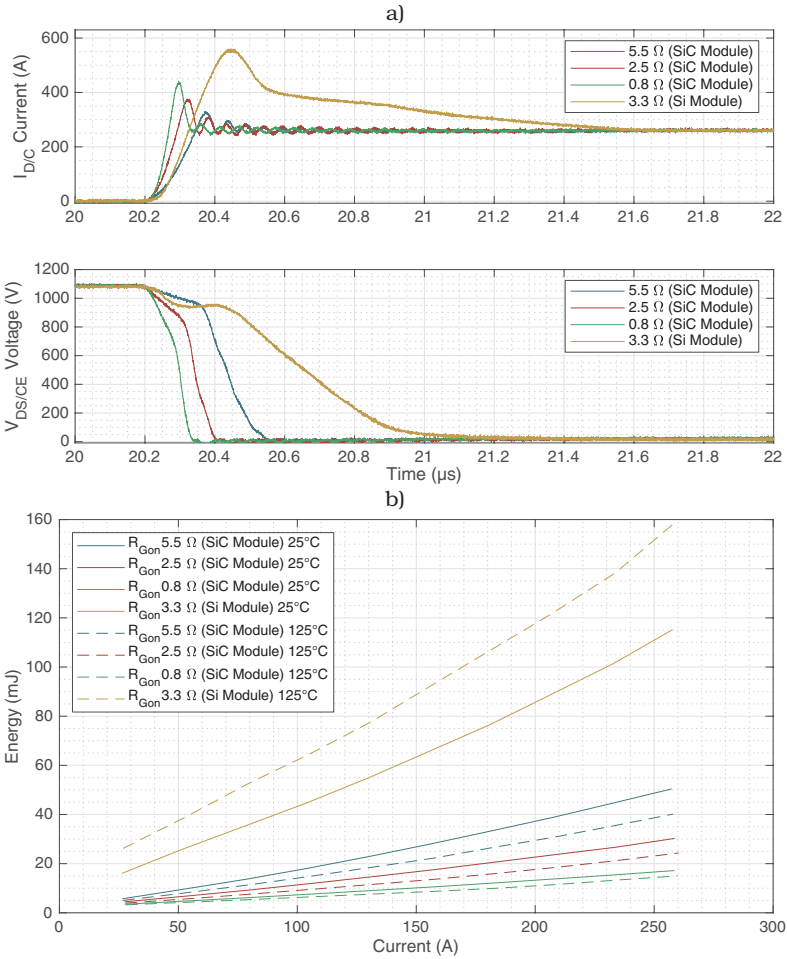


Figure 3.31: Turn-on transient and energy comparison between the SiC-MOSFET module and the Si-IGBT module at V_{DS} = 1100 V. a) Turn-on transient signal comparison at 125°C. b) Turn-on switching loss comparison.

In Fig. 3.31, a comparison of the turn-on transient and energy calculation is presented. There it is possible to observe that the total turn-on time is always slower in the Si-IGBT module for all compared resistances in the test (although it should be noted, that it is even slower that the slowest turn-on resistance presented in this work (8.25 Ω)). Furthermore, when the SiC module uses 5.5 Ω of turn-on gate resistance, the total switching time is lower, even though the current rise time was faster in the IGBT. This is because the voltage fall time t_{fv} is much faster on the SiC-MOSFET than on the Si-IGBT, and as mentioned in the timing values section of the characterization analysis, this fact is overlooked in datasheets as they usually present only current timing data. Furthermore, the soft recovery behavior of the Si-Diode generates additional losses on the Si-IGBT as most of this recovery current still overlaps voltage variation. On the other hand, all SiC responses present some form of ringing in the current, as the output capacitance C_{oss} of the non-conducting MOSFET (blocking device) resonates with the added observed stray inductance (from the switch perspective) of the module plus circuit stray inductance. On the other hand, it can be clearly observed that, regarding turn-on switching loss, the Si-IGBT presents, contrary to SiC-MOSFETs, increased loss depending on temperature. Furthermore, using recommended values, these losses range between 2 and 8 times higher than the SiC based module for the shown gate resistances.

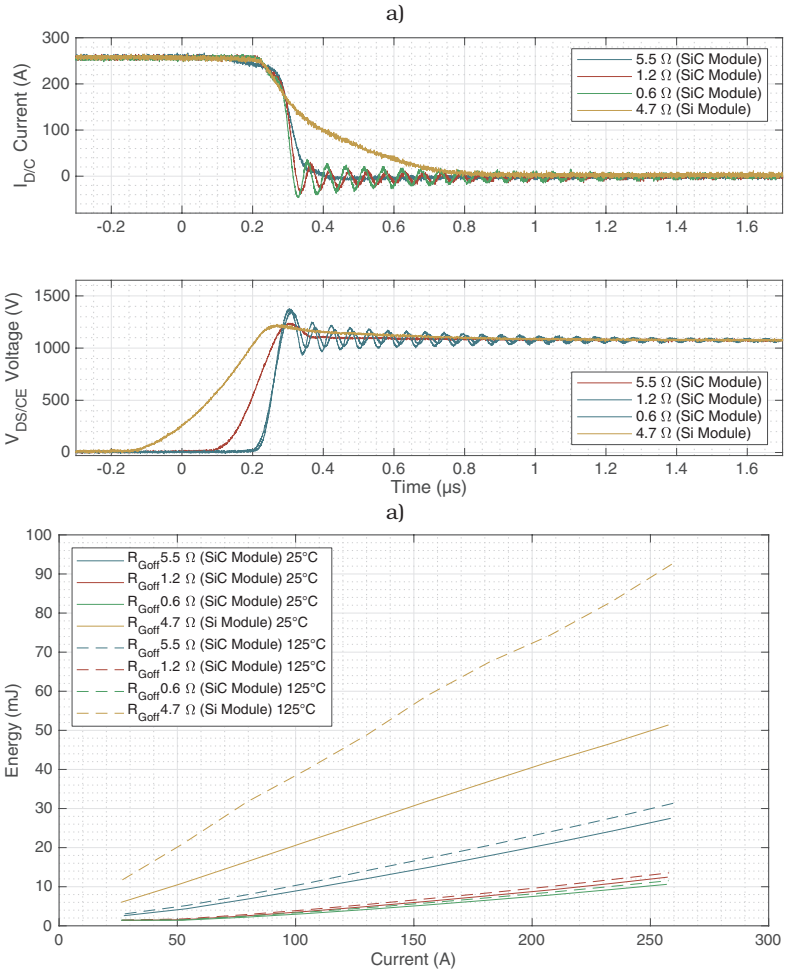


Figure 3.32: Turn-off transient and energy comparison between the SiC-MOSFET module and the Si-IGBT module V_{DS} = 1100 V. a) Turn-off transient signal comparison at 125°C. b) Turn-off switching loss comparison.

When observing the turn-off transient curves in Fig. 3.32, the tail current of the Si-IGBT makes the overall commutation time slower when compared with the SiC device as a result of minority carriers leaving the n-drift region. This current results in 4 times slower current fall time when compared to the slowest $R_{G(off)}$ in test. Furthermore, the switching event on the SiC-MOSFET can be slowed to such extent, that the observed resonance is not excited and the signal turns off smoothly, presenting a total switching time that is still lower than the one observed on the Si-IGBT turn-off event. When comparing energy curves, both devices present additional loss with temperature, but the effect SiC-MOSFETs observe is dwarfed in comparison to the Si-IGBT, which can almost double the loss difference between 25 and 125°C. Furthermore, Si-IGBT turn-off loss using recommended values are between 2 and 9 times the losses obtained with the SiC module with the tested set of $R_{G(off)}$ resistances.

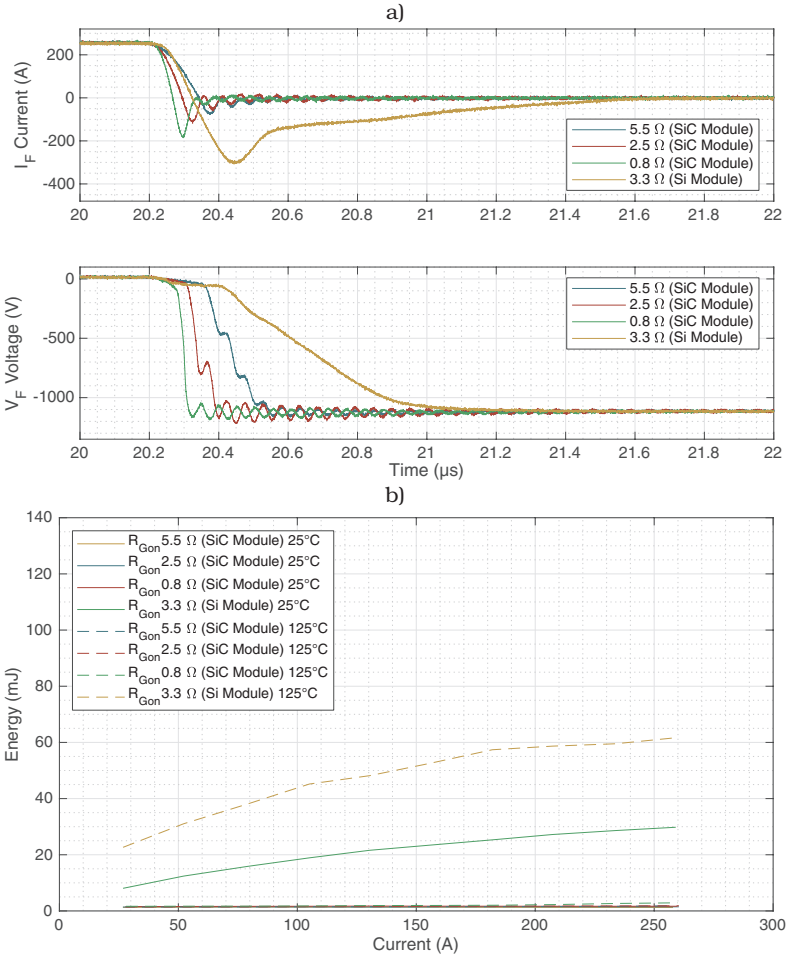


Figure 3.33: Diode turn-off transient and energy comparison between the SiC-MOSFET module and the Si-IGBT module V_{DS} = 1100 V. a) Diode turn-off transient signal comparison at 125°C. b) Diode turn-off switching loss comparison.

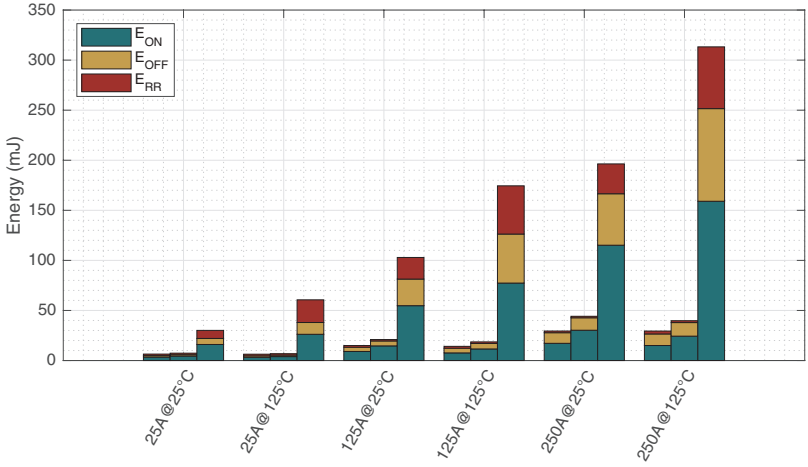


Figure 3.34: Comparison of overall switching losses for three design scenarios and a blocking voltage of 1100 V. Left bar: SiC-MOSFET module with $[R_{G(on)}, R_{G(off)}] = [0.8, 0.6]\,\Omega$. Middle bar: SiC-MOSFET module with $[R_{G(on)}, R_{G(off)}] = [2.5, 1.2]\,\Omega$. Right bar: Si-IGBT module with $[R_{G(on)}, R_{G(off)}] = [3.3, 4.7]\,\Omega$. Losses are shown in function of driven current and junction temperature.

Diode turn-off characteristics can be found in Fig. 3.33. As it can be observed in the figure, the soft-turnoff current characteristic of the Si-diode shares a big overlap area with the diode voltage. This effect is not observed in SiC Schottky diodes, as these devices are unipolar devices, (as seen in chapter 2), and therefore only need to discharge their junction capacitance. As it can be observed in the corresponding loss curves, this has a huge impact in reverse recovery energy. The Si-diode not only dwarfs the SiC-Schottky reverse recovery loss, but is also temperature dependent. This energy comparison is what makes manufacturers advertise their SiC-diodes as zero reverse recovery diodes, but is not exactly zero, as it has been measured here.

Finally, to get an overview of the overall energy loss difference, a summary of the total Si-IGBT module switching energy loss and the total SIC-MOSFET module switching energy loss with gate resistances $[R_{G(on)}, R_{G(off)}] = [0.8, 0.6]\,\Omega$ and $[2.5, 1.2]\,\Omega$ has been made, and it is presented in Fig. 3.34. Here it can be observed that the overall switching loss of the Si-IGBT module is much higher than the SiC-MOSFET module, being up to 10 times higher under full load conditions. Therefore, in order to present similar efficiency, the Si-IGBT module must be operated with slower switching frequencies than the SiC-MOSFET, while taking full advantage of conductivity modulation to reduce conduction loss. This Si-IGBT module presents slightly lower conduction loss at $I_C = 250\,A$ when compared with the SiC-MOSFET module due to this effect. However, due to its knee (saturation voltage), it does not present a quadratic loss dependence on current, but is closer to a linear one, therefore presenting additional conduction loss than a similar SiC-MOSFET for partial load scenarios.

Analysis of dynamic behavior

In Fig. 3.35, the dynamic behavior of the modules at switch turn-on is shown. First of all, in Fig. 3.35.a it can be observed that in the Si-IGBT the di/dt is fairly independent from both load current and temperature, opposite to what its observed in SiC-MOSFETs, where the di/dt increases with both temperature and load current. In Fig. 3.35.b, it can be observed that the Si-IGBT and the SIC-MOSFET present a similar dependence on load current, but opposite in temperature. Both devices decrease the switch dv/dt as current increases (a partial explanation could be the increase in di/dt, which slows down the turn-on due to the source parasitic inductance voltage drop and its effect on the gate loop), but present opposite behavior with temperature, as the Si-IGBT decreases dv/dt with increased temperature instead of increasing it, as it can be observed for the SiC-MOSFET. This effect could be concerning when observing crosstalk or parasitic turn-on effects, but its overshadowed by the dv/dt behavior of the diode. As it can be observed in Fig. 3.35.c, the dv/dt behavior of both diodes is opposite. The Si-IGBT decreases diode dv/dt during diode turn-off (or switch turn-on) for increasing temperature and load current. This makes it less likely to present any miller-capacitance related effects due to this event. However, when observing the SiC-SBD dv/dt, it can be seen that both temperature and load current increase dv/dt, and furthermore, produce the highest dv/dt events in the module (being over 10 times higher than the compared Si-IGBT module). Hence, this dv/dt should be kept in check to avoid electromagnetic issues and crosstalk effects. Common mode transient immunity from drivers and optocouplers in the gate unit should comply with the expected dv/dt at the maximum operation points. Note that the dv/dt presented in this figure presents worse values than the same figure in the paper for the fastest turn-on gate resistance. This is due to an improvement in the dv/dt calculation algorithm that was introduced after the paper was written, as the parallel connected modules presented high dv/dt that showcased the limitations of the algorithm. Nonetheless, the conclusions remain the same, and both dv/dt calculations (old and improved) present worse values than the standard calculation methods, as these track the maximum dv/dt along the curve, instead of only dividing voltage over time using the 10-90%, 20-80% or the 30-50% values using for rise/fall time calculations.

Finally, in Fig. 3.36, the dynamic behavior of the modules at switch turn-off is show. First of all, in Fig. 3.36.a the switch di/dt during turn-off can be observed. Both devices behave similarly, increasing di/dt with load current, but decreasing it with temperature. In other words, the worst case of di/dt during turn-off is at low temperatures, being the MOSFET up to approximately 4 times higher than the IGBT for the presented curves. Since this di/dt increases the peak voltage on the dies due to the power loop parasitic inductances, the low temperature high current operation point plays an important role in designing the nominal operation point of a potential converter using these modules. Finally, in Fig. 3.36.b both devices present increased dv/dt as load current increases. The Si-IGBT dependency though is very small, in contrast with the SiC-MOSFET, which increases with load current, but with a decreasing rate as load current increases. Both devices the increase in temperature results in lower dv/dt during the switching event.

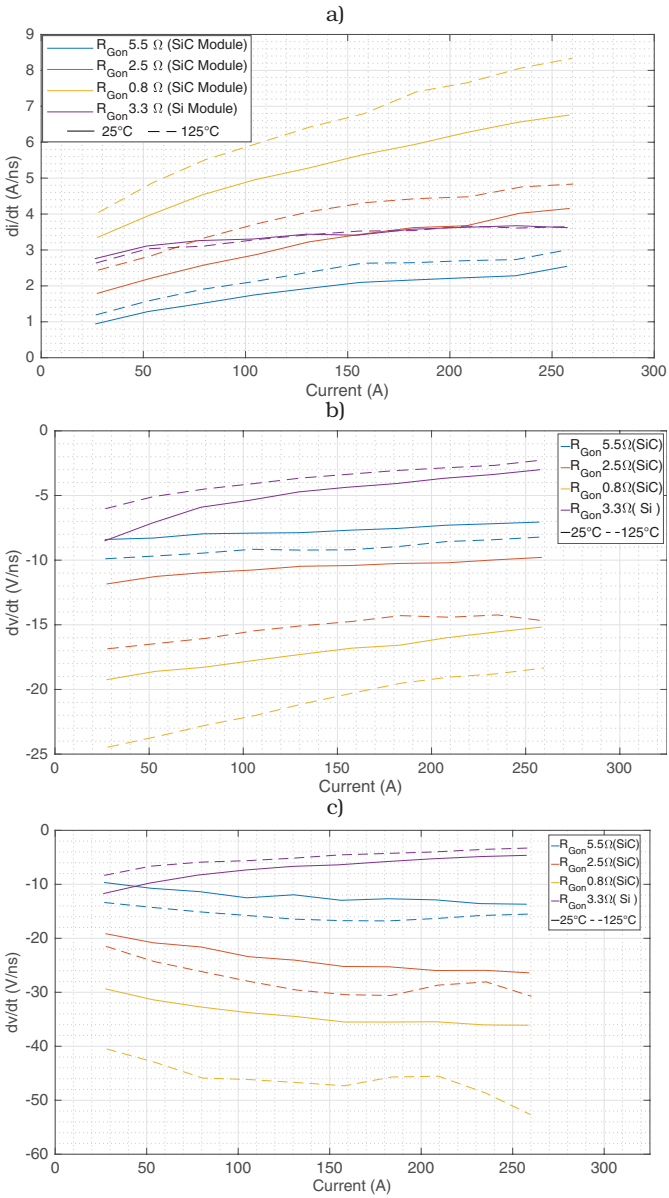


Figure 3.35: Dynamic behavior of the Modules during Switch (SiC-MOSFET/Si-IGBT) Turn-on using different $R_{G(on)}$ gate resistances at V_{DS} = 1100 V and T_J = 25°C and T_J = 125°C. a) Switch di/dt vs current. b) Switch dv/dt vs current. c) Diode dv/dt vs current. ©2019 IEEE. Source: [16].

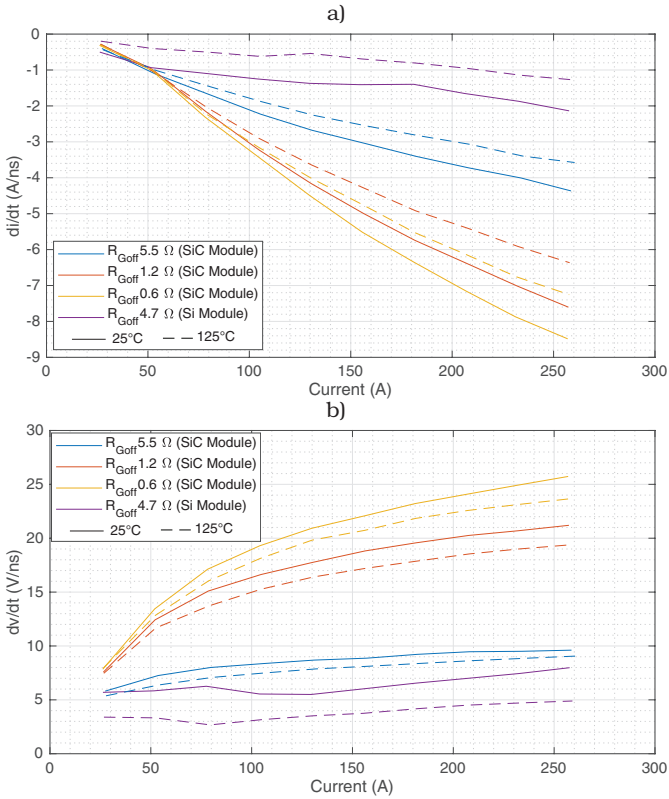


Figure 3.36: Dynamic behavior of the Modules during Switch (SiC-MOSFET/Si-IGBT) Turn-off using different $R_{G(off)}$ gate resistances at V_{DS} = 1100 V and T_J = 25°C and T_J = 125°C. a) Switch di/dt vs current. b) Switch dv/dt vs current. ©2019 IEEE. Source: [16].

Table 3.12: Cases to study loss in both semiconductor modules. ©2019 IEEE. Source: [16].

Case	**Module**	$R_{G(on)}$	$R_{G(off)}$
Case I	SiC-MOSFET module	0.8Ω	0.6Ω
Case II	SiC-MOSFET module	2.5Ω	1.2Ω
Case III	Si-IGBT module	3.3Ω	4.7Ω

Table 3.13: Simulation I main parameters. ©2019 IEEE. Source: [16].

Parameter	Value
DC-link Voltage	1100 V
Load Current I_L	250 Sin(2π50t) A
Case temperature T_c	80°C
Modulation index	1.1547
Power Factor	[-1, 1]
Frequency range	[1 50] kHz

Simulated comparisons of modules with fixed case temperature

With the experimental data obtained from the characterization of their dynamic characteristics, and complimented with static data from their forward characteristics and transient thermal impedance curves, simulation models to be used in PLECS have been implemented to study how these devices would fare in a three-phase two-level voltage source inverter connected to the grid. Both models have been implemented in PLECS as described in Fig. 3.37.a, in which a single leg is modeled and modulated to estimate the corresponding losses and junction temperatures in the corresponding devices. To determine the junction temperatures on the devices, the thermal impedance of the corresponding modules has been used (usage of thermal impedance curves for junction temperature estimation is described in section 4.2.2: Thermal Modeling).

These models have been used in two simulations scenarios with the following goals:

- to observe loss and junction temperature variations for fixed sinusoidal currents at fixed case temperature in function of switching frequency, and
- to estimate the maximum sinusoidal current amplitude that can be driven through the modules at fixed case temperature in function of switching frequency.

This is performed for three proposed design cases, use the SiC-MOSFET module with the fastest resistance pair in study, use a more conservative configuration of the SiC-MOSFET module, or use the Si-IGBT module with the recommended resistance pair proposed by the manufacturer. These cases are summarized in Table 3.12.

In the first simulation, the conditions of the experiment are described in Table 3.13.

In the second simulation, the case temperature is fixed for 80°C as well, for

the same power factors and modulation index, but now the peak current that generates the critical condition of having all junction temperatures just below 125°C is plotted against switching frequency.

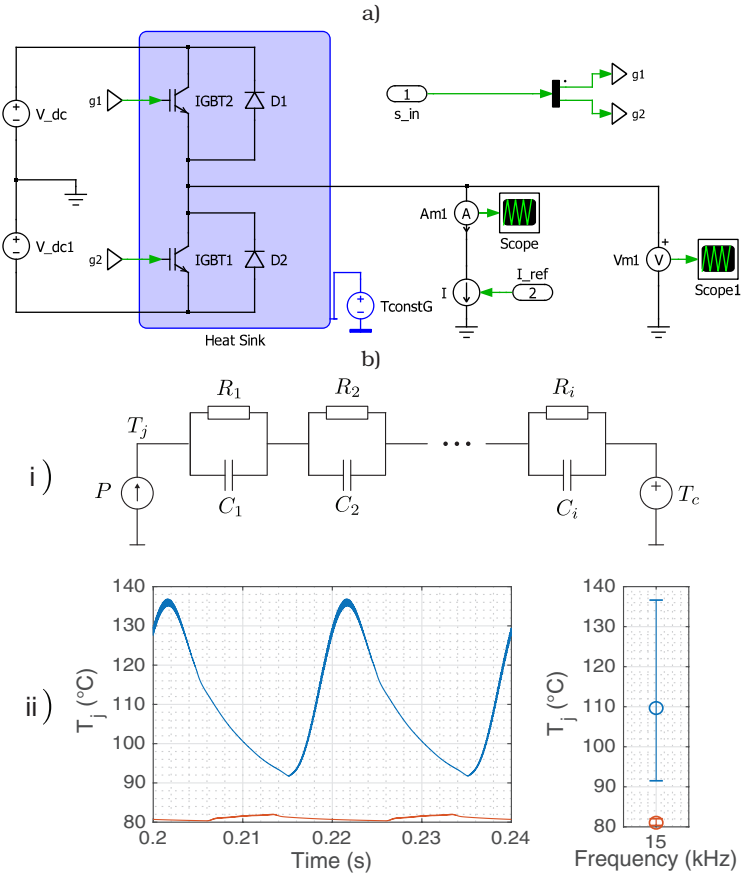


Figure 3.37: Simulation scheme to perform the study of loss, current and junction temperatures on the Modules. a) PLECS based simulation to compute module losses and junction temperatures in converter using a fixed case temperature. b).i Foster thermal model of i stages to calculate the junction temperature variations. b).ii Example of the summarized junction temperature variations. Left: Temperature variation of SiC switch and SBD in steady state during two 50 Hz current cycles while modulated at 15 kHz. Right: Summary of the time domain temperatures as maximum, minimum and average junction temperature values as a function of frequency for the shown temperatures. ©2019 IEEE. Source: [16].

In Fig. 3.38.a, the loss comparison of the three cases described in Table 3.12 are presented. Regarding conduction losses, it can be observed how the Si-IGBT module presents lower values than the SiC-MOSFET module due to conductivity modulation even though it is a thicker device for the same blocking voltage. This advantage of conduction losses though only happens at nominal current, because at lower loads the knee voltage of the Si-IGBT decreases its efficiency in comparison with the SiC-MOSFET module. On the other hand, when observing switching losses, as soon as the switching frequency rises over 3 kHz, the Si-IGBT module losses at least double the overall losses of the SiC module for the same frequency, being comparable with SiC device losses when these switch almost 10 times faster. Furthermore, the diode recovery loss plays an important role in the overall losses in the Si-IGBT module. This effect is negligible in the SiC module due to the unipolarity of the SiC SBD. As final remark: the maximum dissipation of the package is 1800 W, and therefore the Si-IGBT module could only work up to 7 kHz operating under these simulation conditions. On the other hand, the SiC-MOSFET module also presents a current limitation in this example, but it is result of a temperature limitation, as it can be seen in Fig. 3.38.b. This temperature increase is also accountable for the increase in $R_{DS(on)}$ at higher frequencies, hence explaining the increase in conduction losses.

Referring to junction temperature oscillation range with PF = 1, it is shown in Fig. 3.38.b. that the differences between maximum and minimum junction temperature in the Si-IGBT are smaller than on the SiC-MOSFET despite the additional loss. The main reason is that since SiC has a higher current density capability, less material is used to drive the same current, and therefore the chip area is smaller than a competitor Si-IGBT of the same ratings. Hence, the SiC-MOSFET presents a smaller thermal capacitance and therefore, presents higher thermal oscillation amplitudes in comparison with the Si-IGBT. Additionally, since the SiC-Diode does not present significant reverse recovery losses, stays cool in comparison with a standard Si-Diode and its corresponding SiC-MOSFET, which implies that the module could be reduced in size to make it cheaper if i^2t or other diode dependent criteria is not needed by potential module customers.

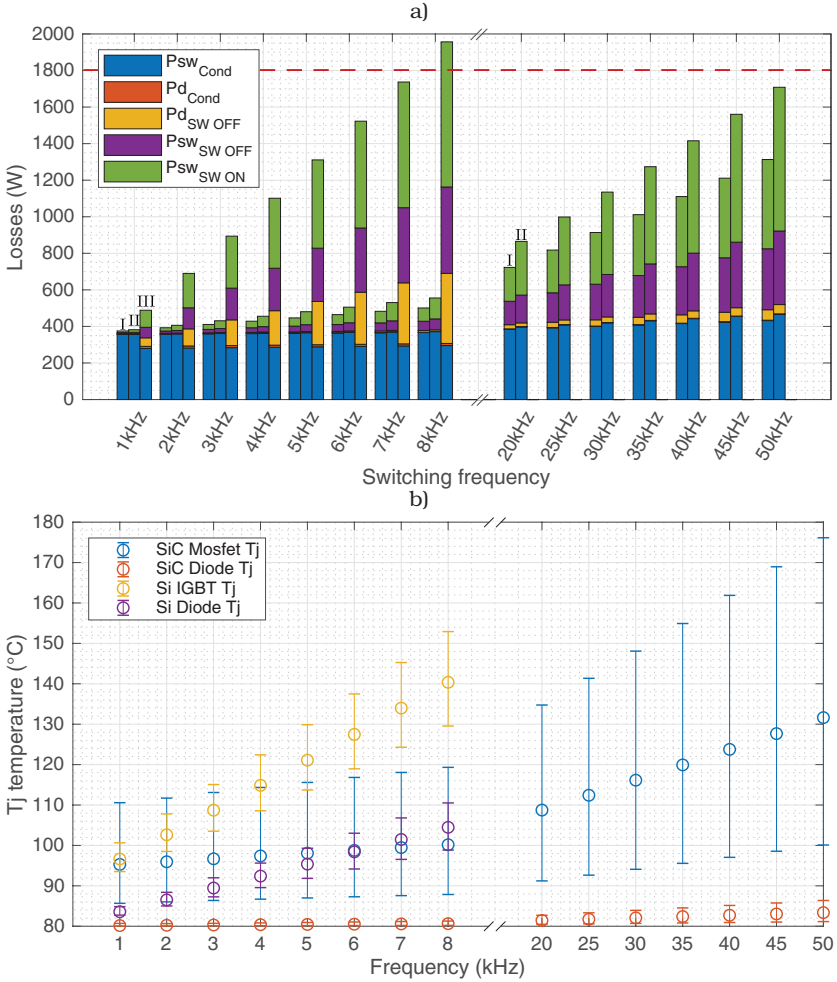


Figure 3.38: Loss and junction temperature comparison between the modules for the cases I, II and III vs frequency, for V_{DC} = 1100 V , I_L = 250 A, M = 1.1547 and PF = 1. a) Loss comparison vs switching frequency for the cases I, II and III b) Junction temperature variations for cases I and III vs frequency. ©2019 IEEE. Source: [16].

When observing the loss distribution with PF = -1, as presented in Fig. 3.39.a, the conduction losses in the case of the Si-IGBT module are due to the diode alone, being the only device capable of driving in current in that direction. On the other hand, the SiC-MOSFET can be operated in active rectification, to use its channel parallel to the SiC-Diode to further reduce conduction losses, and furthermore, since the losses are shared, lower temperatures for each device are reached as well (Fig. 3.39.b). Regarding switching losses, in this case the loss gap becomes more significative: the Si module losses at 2 kHz are already comparable to the losses in the SiC module switching at 20 kHz.

Referring to junction temperature oscillation range with PF = -1 (Fig. 3.39.b), it is observed that since the SiC devices share the current, the devices present both lower average junction temperature and smaller junction temperature oscillations. This enables higher currents and/or higher switching frequency when using operating in rectification mode, as it was observed that the main limitation with PF = 1 was high MOSFET T_J temperature. Special remark here is that the MOSFET is always hotter that the diode, independent on current direction. This makes it the main boundary when defining the maximum current of the module in both in regenerative, and non regenerative operation modes.

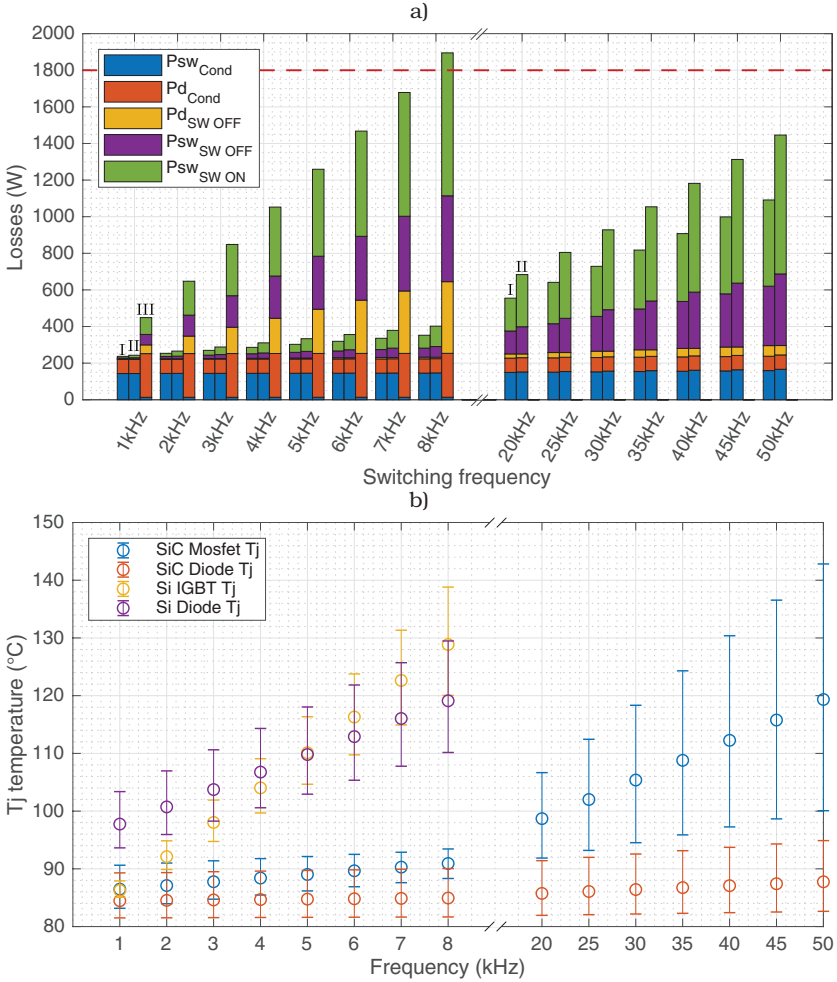


Figure 3.39: Loss and junction temperature comparison between the modules for the cases I, II and III vs frequency, for V_{DC} = 1100 V , I_L = 250 A, M = 1.1547 and PF = –1. a) Loss comparison vs switching frequency for the cases I, II and III b) Junction temperature variations for cases I and III vs frequency. ©2019 IEEE. Source: [16].

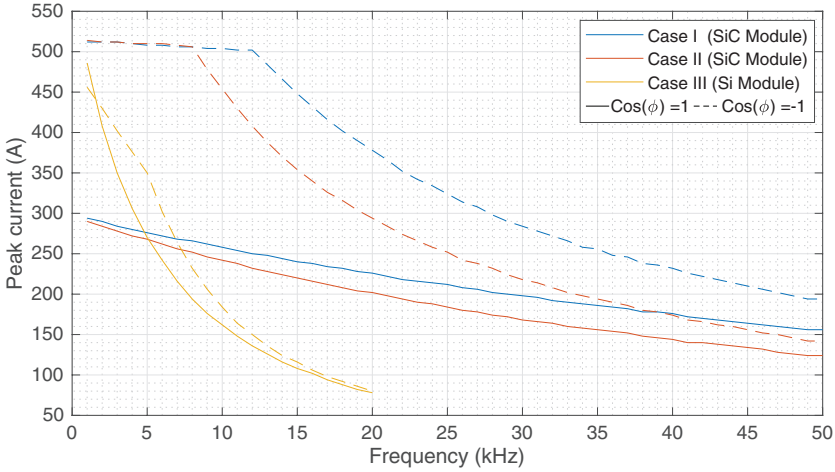


Figure 3.40: Maximum current vs frequency for cases I, II and III considering V_{DC} = 1100 V, M = 1.1547 and power factors PF = {−1, 1}.©2019 IEEE. Source: [16].

Finally, the results of the second simulation can be observed in Fig. 3.40. There it is observed that at lower switching frequencies with PF = 1, the Si-IGBT module is able to drive close to 60% more current than the SiC module due to its lower on-state losses. However, over 5 kHz the SiC-MOSFET module presents higher current handling capability due to lower switching losses, being able to drive currents of 230 A peak at 20 kHz, over three times the Si-IGBT module driving capability at the same frequency. On the other hand, with PF = -1 both devices present a decreasing linear behavior first, which is mainly driven by diode or diode plus channel loss. Afterwards, switching loss becomes the significant factor to drive the junction temperature, at which point the linear behavior breaks into a convex function. Overall, the Si-IGBT module presents a balanced behavior between both power factors, which is hard to match for SiC module designers as they need to balance this behavior in a wider frequency range and gate resistor combinations. Furthermore, the balance of SiC-MOSFET chip area and SiC-Diode chip area requires optimization for different frequencies as well.

These results are nonetheless considered preliminary comparison, as a full comparison of both modules in converter operation is performed in chapter 5.

3.2.7 Single Module Results Summary

The DUT was analyzed through double pulse tests and forward measurements and both its transients and on-state behavior has been measured and characterized. From the obtained results, the main conclusions remain the following:

- The SiC-MOSFET module can switch for up to 30.5 mJ total loss energy at V_{DS} = 1100 V by using the lowest gate resistance pairs in study.
- The fastest observed turn-on time under full load condition and lowest $R_{G(on)}$ at V_{DS} = 1100 V was 114 ns, or 176 ns if turn-on delay is considered.
- The fastest observed turn-off time under full load condition and lowest $R_{G(off)}$ at V_{DS} = 1100 V was 65 ns, or 268 ns if turn-off delay is considered.
- The highest observed reverse recovery loss was 4.1 mJ, with $R_{DS(on)}$ = 0.8 Ω, V_{DS} = 1100 V, and T_J = 125°C.
- Diode dv/dt was the highest dv/dt on study, and it is the main parameter to observe for dv/dt related issues in half-bridge operation. It has also been observed that with the smallest turn-on resistance this value is close to the 50 V/ns the manufacturer has tested without observable failure mechanism effects. For this reason, no smaller turn-on resistance as the recommended by manufacturer has been used in further tests (1 Ω). Furthermore, and as previously explained, since this device will be operated in parallel connection, the module nominal current will not be reached, and therefore the observed dv/dt was expected to be lower.

Regarding the experiments themselves, the main conclusions were the following:

- Common mode current paths must be carefully considered in gate unit design because of the coupling capacitances that are present in isolation barriers and DC/DC converters in charge of powering them.
- The measurement of the gate voltage considering the switching voltages and the required accuracy during transients is a problem in itself, and a better method to measure this quantity would be very useful to observe if there are effectively parasitic turn-on events, and to be able to accurately relate observed effects between power signals and gate voltage.

Finally, a short summary of basic observed effects depending on the most important variables is depicted for both the MOSFET and the diode in Tables 3.14 and 3.15 respectively.

Table 3.14: Summary of observed effects in the SiC-MOSFET depending on the increase of main variables.

	MOSFET turn-on			MOSFET turn-off		
↑ T_J	↓ t_{ri}, ↓ t_{fv}	= $t_{d(on)}$	↑ $\frac{dv}{dt}$, ↑ $\frac{di}{dt}$	↓ $\frac{dv}{dt}$, ↓ $\frac{di}{dt}$	↑ t_{ri}, ↑ t_{fv}	↑ $t_{d(off)}$
↑ I_D		↑ $t_{d(on)}$	↑ t_{ri}, ↑ t_{fv} ↑ $\frac{dv}{dt}$, ↑ $\frac{di}{dt}$	↓ t_{fi}, ↓ $t_{d(off)}$ ↓ t_{rv}		↑ $\frac{dv}{dt}$, ↑ $\frac{di}{dt}$

Table 3.15: Summary of observed effects in the SiC-diode depending on the increase of main variables.

	Diode turn-off
$\uparrow T_j$	$\uparrow \frac{dv}{dt}, \uparrow \frac{di}{dt}$
$\uparrow I_F$	$\uparrow \frac{dv}{dt}, \uparrow \frac{di}{dt}$

3.3 Characterization of the Parallel Connection of the 1700 V 250 A SiC Module

3.3.1 Motivation and Fundamentals

In contrast with the single device characterization procedure, the parallel characterization of SiC modules does not focus in device characteristics, but in their interaction and their operation as a single power block unit. Therefore, the main objectives of this characterization are:

- Characterize the current sharing behavior of the parallel-connected modules.
- Analyze the switching loss sharing behavior of parallel-connected devices.
- Obtain relevant information for driving purposes.

To that end, both previously mentioned testbenches have been used in order to shed light over these unknowns.

3.3.2 Testbench Configurations for the Characterization of Parallel-connected Modules

The parallel connection of two modules can be performed in several ways. For example by having individual gate units for each switch, for each module, a single driver for the two modules or something in between. In this case, the concept was to use a single driver with two output stages, while directly connecting the kelvin sources (sources for the driving circuit) to ensure balanced parallel switching behavior while simplifying timing and communication requirements. Exploring this parallel concept, the gate units GUV2 and GUV3 were developed, and the DPT testbench was slightly modified by introducing a modified version of the copper plates to allocate the two modules symmetrically from the center. In Fig. 3.41, the physical connection of the parallel-connected modules featuring the GUV2 can be observed.

The load inductor is a 150 µH air coil, which value was verified through an impedance meter. This inductance was reduced from the 380 µH to require less initial voltage on the DC-Link while loading more current in the load inductor to characterize the parallel behavior of the modules, while also providing reasonable pulse times and acceptable currents at the end of the second pulse.

Both gate unit measurement scheme concepts are presented in Figs. 3.42 and 3.43 for the gate units GUV2 and GUV3 respectively. As it can be observed in both schemes, a negative voltage power source has been used (instead of the

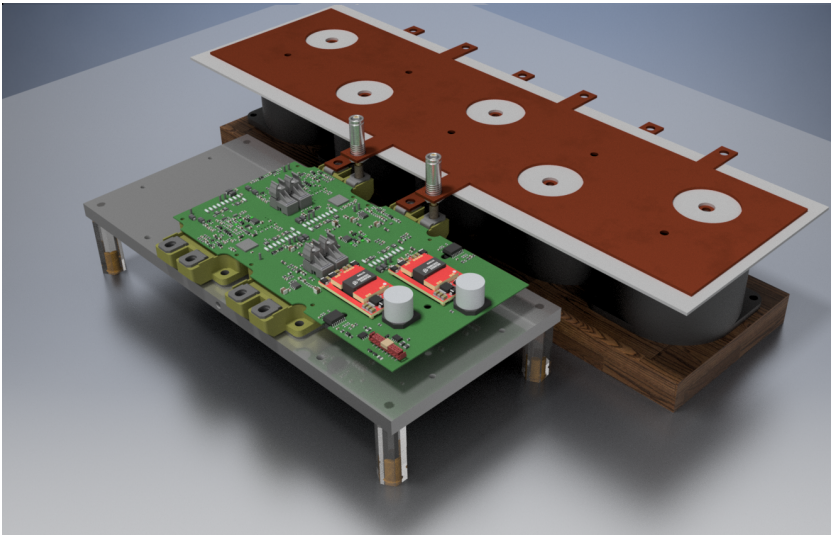


Figure 3.41: DUT cell for parallel connection, featuring DC-Link copper plates for symmetric parallel connection of modules and the second version of the gate unit (GUV2).

positive voltage source that was used in the single device characterization experiments) to set the DC-link voltage for the DPT event. This is because the shunt resistors need to be grounded, as they ground the oscilloscope through the ground of the BNC cable. The alternative of putting the shunts in the sources was disregarded as it could lead to wrong results due to the possibility of currents flowing through the kelvin source between the modules. This effect is completely avoided when measured in the drain of the upper MOSFETs, as there all measured current (either for MOSFET or diode) must have flown through their corresponding module. The main disadvantage from this measurement scheme is that now there is no gate voltage that can be measured close to ground potential, which is a problem in itself as it was explained in the single module measurement. Hence, this voltage was not measured.

For both gate unit concepts, the load inductor is connected either to A or B (see Fig. 3.42) depending on the device that was to be characterized. When connected to A the lower MOSFET is switched and diode characterization is carried out. On the other hand, when connected to B the upper MOSFET is both switched and characterized. The main difference among them is the addition of the turn-off resistances in the kelvin source path, which offers a high impedance path to the current when compared with the MOSFET $R_{DS(on)}$.

Testbench equipment regarding parallel-connected DPT is presented in Table 3.16. The main differences are the usage of a different oscilloscope, the negative voltage power source and the modification of the load inductor value when compared with the single module testbench equipment in Table 3.3.

Finally, probe selection regarding parallel DPT is presented in Table 3.17 where

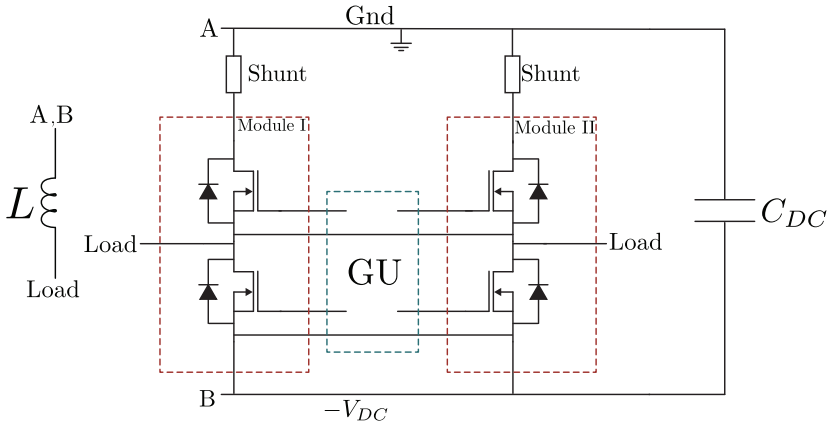


Figure 3.42: Schematic connection for parallel characterization using the GUV2. When the load inductor L is connected to A, diode measurements are performed. When the load inductor is connected to B, MOSFET measurements are performed.

Table 3.16: Testbench equipment for the characterization of parallel-connected modules.

	Testbench
Oscilloscope	Lecroy HDO6054-MS 500 MHz
Power Source	Iseg HPS -2kV 150 mA (HPn)
Control Platform	Xilinx Zynq 7010 SoC
DC-Link	110 µF
Aircoil	150 µH
Hotplate	[25 125]°C

the letter indicates the corresponding module. Most probes remain the same as when characterizing single module behavior, with the sole exception of the Rogowski coil CWT15bmini. Due to its limited bandwidth though, this device cannot be used to characterize device transients, and was instead used in the GUV2 scheme to characterize current distribution while in the on-state of the pulses. On the other hand, on the GUV3 this measurement was not necessary, and was only used as an auxiliary measurement to observe the current through the unmeasured shunt in the oscilloscope during experiments.

3.3.3 Experimental Investigation of the Behavior of Parallel-connected Modules

The transient characterization of parallel-connected SiC modules has been performed by using a single gate resistance pair per gate unit and subsequently performing measurements at 900, 1000, and 1100 V, from currents ranging

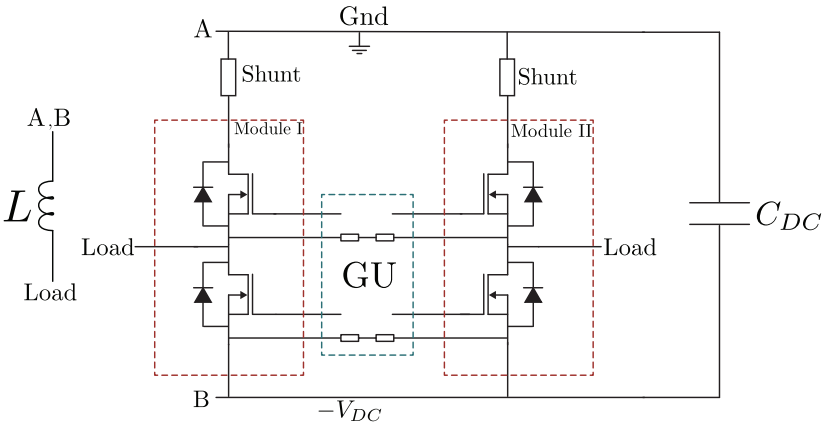


Figure 3.43: Schematic connection for parallel characterization using the GUV3. Kelvin source resistances are included, which limit kelvin source current flow and enable current distribution measurements without the need of Rogowski coils. When the load inductor L is connected to A, diode measurements are performed. When the load inductor is connected to B, MOSFET measurements are performed.

from 100 to 650 A at 50 A intervals, at 25 and 125°C. The reason of only using one pair of resistances for each characterization is the sheer number of DPT events required to fully characterize a single gate resistance pair. These double pulse test events were then analyzed and both timing data and energy loss was also registered. A summary of the performed experiments is presented in Tables 3.18 and 3.19 for the GUV2 and GUV3 measurements respectively.

Regarding the measurements performed with the GUV2, as previously mentioned, currents could potentially flow through the kelvin sources and introduce error in the measurements while possibly leading to long term failure if this current was significant. For this reason, the impedance paths that both modules observe must be as similar as possible. Additionally, shunt resistors are in the range of the $R_{DS(on)}$ resistances of the modules, and therefore could support current distribution while used together. This would lead to a better current

Table 3.17: Measurements and Probes for the characterization of parallel-connected modules

Probes	
$I_{D/f\ A}$	400 MHz Shunt resistor SSDN-414-01
$I_{D/f\ B}$	400 MHz Shunt resistor SSDN-414-01
$I_{D/f\ A}$	15 MHz Rogowski coil CWT15bmini
$I_{D/f\ B}$	15 MHz Rogowski coil CWT15bmini
$V_{DS/F}$	300 MHz Differential probe PKM Bumblebee
I_L	20 MHz Pearson current transformer model 401

Table 3.18: Summary of parameters on the performed DPT over parallel-connected modules using the GUV2.

Parameter	Tested values
V_{DS}	{ 900, 1000, 1100 } V
I_D	100 to 650 A at 50 A steps
T_j	{ 25, 125}°C
$R_{G(on)}$	1.8 Ω
$R_{G(off)}$	1.1 Ω

sharing measurement than what would be measured without the shunts. Hence, a measurement with modules directly connected to the DC-Link was required to measure current distribution. This measurement was performed with Rogowski coils, and although their bandwidth did not allow for trustworthy measurements during transient, through them it was possible to measure current distribution while the devices were in on-state.

An additional measurement problem was that the two shunts could not be measured at the same time because they generated circulating currents through the oscilloscope. Therefore, six rows of measurements per resistance pair were required, 3 for the MOSFET and 3 for the Diode. These are:

1. With both shunts installed, the left shunt is connected to the oscilloscope and the other current is measured through a Rogowski coil. This measurement is used to study switching characteristics of the left module, as during the switching event the resistance is dominated by the MOSFETs and not the shunts.
2. With both shunts installed, the right shunt is connected to the oscilloscope and the other current is measured through a Rogowski coil. This measurement is used to study switching characteristics of the right module, as during the switching event the resistance is dominated by the MOSFETs and not the shunts.
3. With direct connection of the modules to the copper plates (no shunts, but through bronze screws), both channels are measured through Rogowski coils to observe current distribution between the devices. This works because the coils are not subjected to dv/dt by being on the direct path to ground (otherwise the dv/dt generates a coupling effect that introduces error in the measurement).

On the other hand, when using the GUV3, the turn-off resistances have been moved to the kelvin source path. This enables the possibility of measuring current distribution without having to take the shunts out of the circuit thanks to the gate resistances, which present app. 40 times more impedance to the current than the traditional path through the module.

Therefore, for GUV3, the measurement rows are as described for the GUV2, with the difference that the 3rd step (Rogowski coils) was not necessary and the current distribution could be estimated with experiments from the complimentary pulse event, and with the Rogowski coil of the corresponding pulse for verification as the circuit stays the same and the shunts do not influence current distribution. Therefore only four measurement rows per resistance pair were

Table 3.19: Summary of parameters on the performed DPT over parallel-connected modules using the GUV3.

Parameter	Tested values
V_{DS}	{ 900, 1000, 1100 } V
I_D	100 to 650 A at 50 A steps
T_j	{ 25, 125}°C
$R_{G(on)}$	1.0 Ω
$R_{G(off)}$	0.2 Ω

necessary.

Due to the great amount of measurements required to characterize a single resistance pair, only one resistance pair per gate unit has been tested. Therefore, and although most results will focus on the third version of the gate unit as it was the final design to be used in the converter, results obtained with the second version of the gate unit will also be provided, as this information is also insightful from a gate resistance pair perspective.

Current Sharing Behavior of the SiC MOSFET Module

The first analysis regarding current sharing behavior between modules was performed using the second version of the gate unit (GUV2 and $R_{G(on)}$ = 1.8Ω, $R_{G(off)}$ = 1.1Ω). This analysis was performed during the DPT events and is presented in Fig. 3.44. There it can be observed that between diodes and MOSFETs, the diodes are most suggestible to uneven current distribution. Temperature also affects transient current sharing negatively, being the worst measured current difference 80 A for the Diode for a 650 A total driven current at T_J = 125°C and V_{DC} = 1100V. Please note that this measurement is only referential, as shunts could be helping with current distribution.

For practical purposes, it should be remembered that parallel connection of modules require certain derating, and therefore it is expected that the final design should drive an approximated maximum of between 400 and 450 A_{peak} as the module nominal current is 250 A@60°C. This would position the worst total current difference at close to 30 A during transient and on-state, being the diodes the critical element. Additionally, it should be considered that both the diode and the MOSFET present positive temperature coefficient between resistance and temperature. In other words, when one device drives more current, heats up and its resistance rises, which acts as a negative feedback loop, autobalancing current distribution. This effect cannot be observed here as the total DPT event lasts maximum 200 µs considering the loading ramp, which is not enough time to heat up devices significantly.

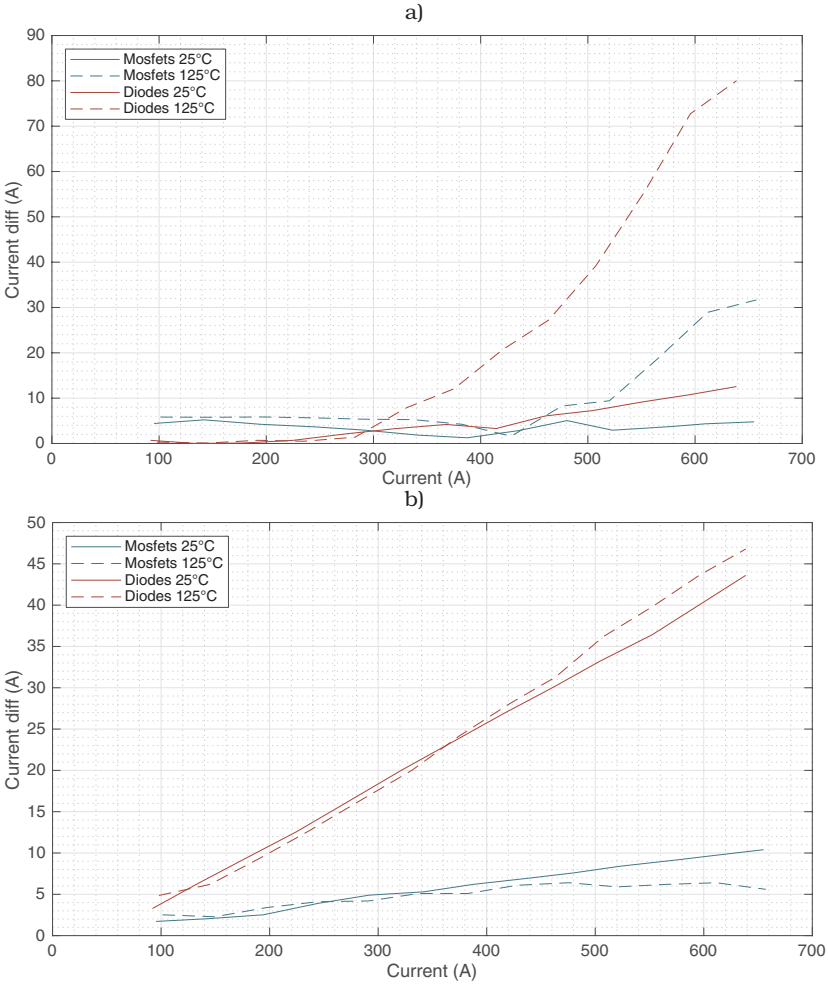


Figure 3.44: Difference of driven currents between modules vs total driven current while using the GUV2 at V_{DS} = 1100 V. a) Peak current difference between MOSFET turn-on transient current and diode reverse recovery currents using shunt resistor measurements of their corresponding DPT events. b)Max. current difference among MOSFETs and diodes during the 2-10 µs part of the respective turn-on time for both devices using Rogowski coil measurements (in the same DPT event).

On the other hand, the current source testbench was also used to characterize current distribution while using the GUV2. In this case, only Rogowski coils were used, to avoid risk influencing current distribution with the shunts. These results are presented in Fig. 3.45 (MOSFET values are not presented, as they were less than 5 A apart). From the results, it can be observed that the diode behaves similarly when compared with DPT on-state results, presenting a small reduction when observed in this longer timeframe, and staying below the 15 A difference for 250 A per device current. On the other hand, when observing current sharing among modules when also using the MOSFET channel in 3rd quadrant mode, the current unbalanced increased. However, current difference values stay below the 25 A, and the extra current taken by one of the modules is then distributed among devices, which results in less current through the diode than in the case of operating without the parallel channel.

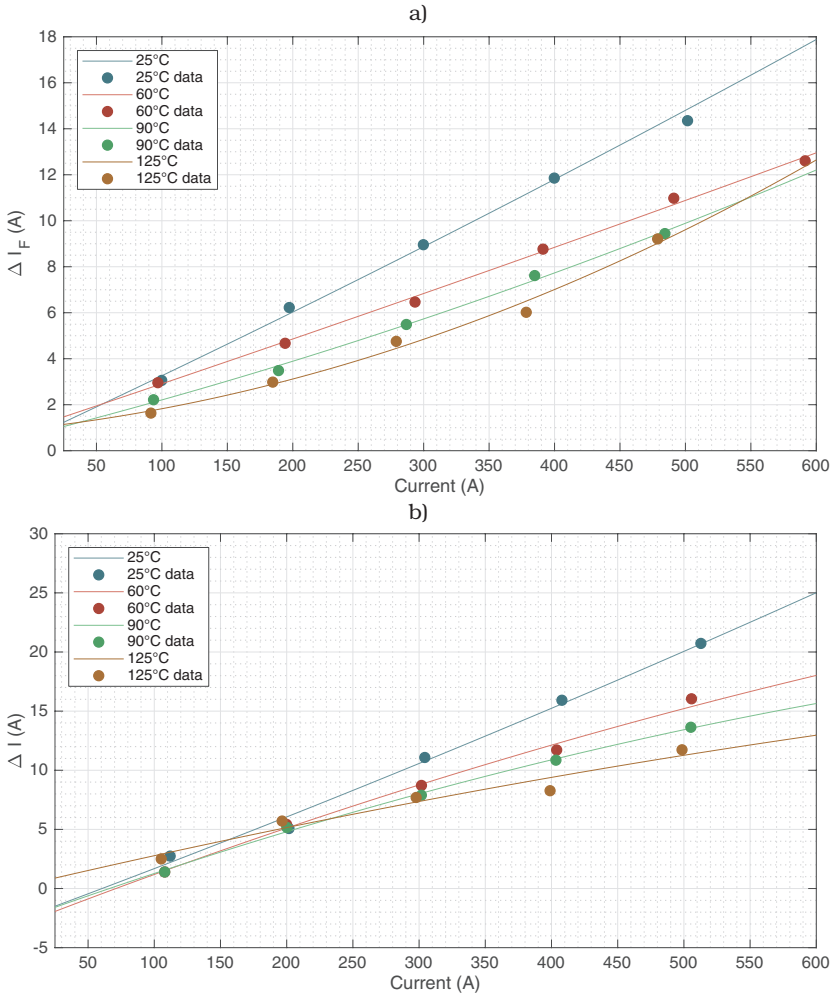


Figure 3.45: Current sharing between the modules at the 2 ms mark vs total driven current while using the GUV2. a) Diode current sharing. b) Diode + MOSFET channel current sharing.

However, the main problem of the GUV2 was that there was not a reliable way to ensure that the current flow through kelvin sources was, and would remain, within safe margins. An internal inspection of a burnt module provided the possibility to estimate that these kelvin source pins should be able to reliably operate with a steady current of less than 10 A. Therefore, the third version of the gate unit (GUV3) included the turn-off resistors in this path, so now it was possible to measure the voltage drop over these resistors to observe this current. The results of this measurement are presented in Fig. 3.46, and as it can be observed, remain below 2 A in average, which is within safe margins.

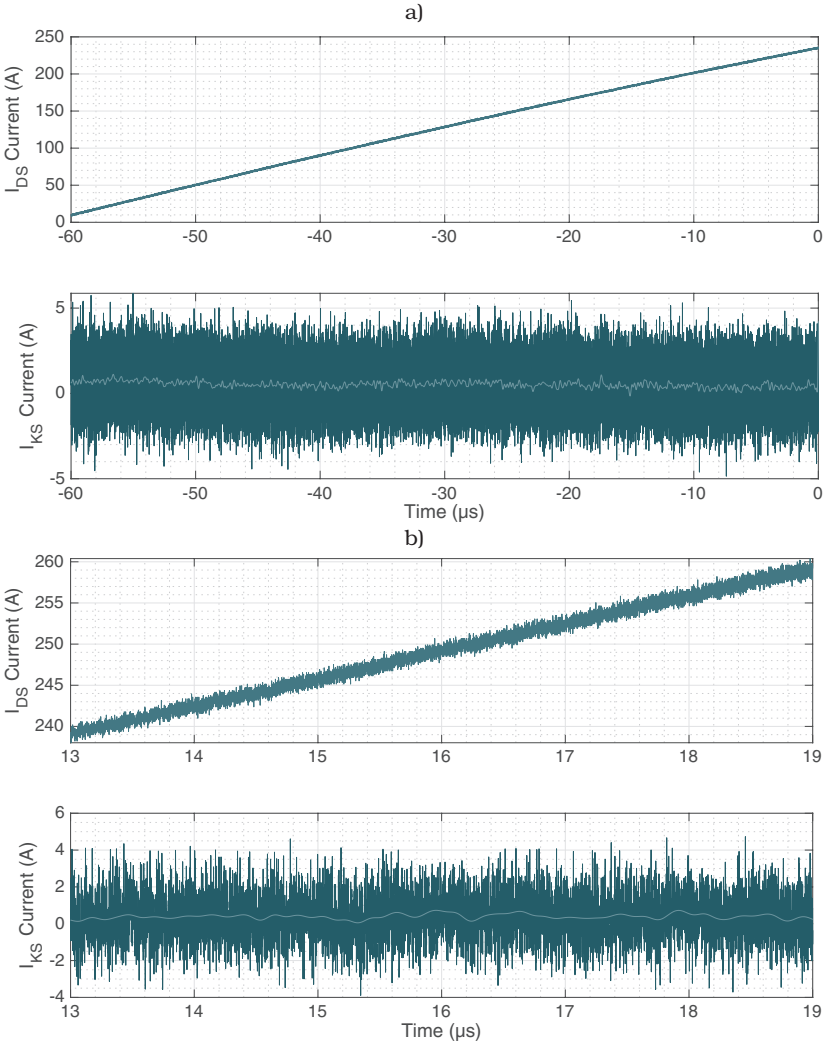


Figure 3.46: Measured current through the Kelvin source during turn-on using the GUV3. The current was measured by measuring the voltage drop over the turn-off gate resistance of the kelvin source. a) I_{DS} current and the measured current through the Kelvin source during the first pulse (current ramp charging the load inductor). b) I_{DS} current and measured current through the Kelvin source during the second pulse (10 µs Turn-on pulse).

Therefore, like with the second version of the gate unit (GUV2), current sharing was also analyzed for the GUV3, but this time with datasheet recommended gate resistance values ($R_{G(on)}$ = 1 Ω, $R_{G(off)}$ = 0.2 Ω), and results can be found in Fig. 3.47. In it, it can be observed that the maximum current difference during on-state got reduced when compared with GUV2 results. On the other hand, peak transient current differences among devices is significantly higher than the results obtained with the GUV2 and its resistance pair. However, below 400 A these differences are not as critical, and the highest current would still be within margins of the rated pulsed current of the modules (500 A). Additionally, the associated switching loss among devices due to this difference remains small. This is further discussed in the next section.

Finally, forward measurements have not been performed for the GUV3 as it presents better current sharing behavior in the turn-on state of the DPT tests (as it can be observed in Fig. 3.47) and since gate unit resistances do not influence forward characteristics, no big differences with the GUV2 tests were expected.

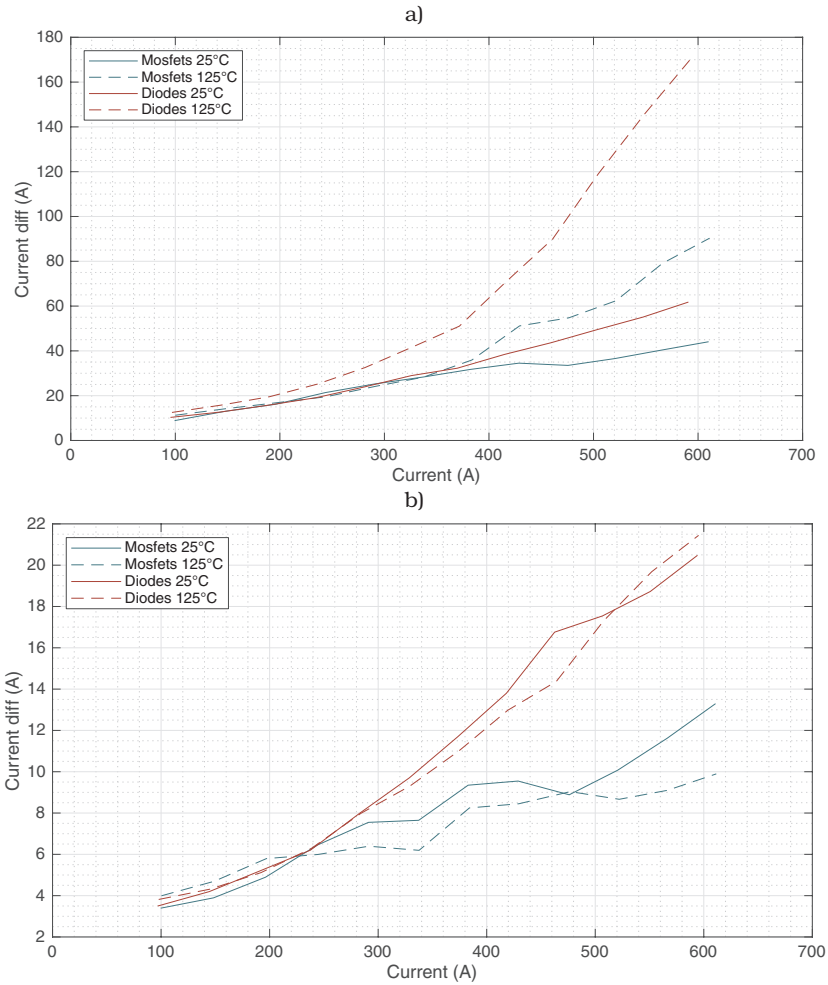


Figure 3.47: Difference of driven currents between modules vs total driven current while using the GUV3 at V_{DS} = 1100 V. a) Difference between MOSFET turn-on transient peak current and Diode reverse recovery currents using shunt resistor measurements of their corresponding DPT events. b) Max. current difference between MOSFETs and Diodes during the 2-10 µs part of the respective turn-on time for both devices.

Switching Loss Distribution among SiC-MOSFET Modules

As observed in current sharing experiments, current sharing during on-state is quite balanced relative to the driven current amount. However, since current sharing during transients can present major differences among devices depending on the driven current, it was of interest to observe the corresponding loss distribution this uneven behavior generates.

In Fig. 3.48 the turn-on switching loss distributions for both gate unit resistance pairs (hence using GUV2 and GUV3) for module A (left module) and module B (right module) are presented. First point to remark is that results are in the expected range when compared with single module results, however, they present different switching loss distribution among modules. Particularly regarding the GUV3, this difference is close to 4 mJ in worst case scenario, being slightly reduced at high junction temperature T_J = 125°C. Due to the higher current difference between MOSFETs at T_J = 125°C, a higher loss difference would be expected. However, the peak current occurs when an important amount of the blocking voltage has already dropped, and this added to the loss reduction the devices present when switched at higher temperatures are the main explanations that have been found for this effect. On the other hand, for the GUV2, MOSFET current sharing during transient is less than half of the observed current difference in the GUV3 (the gate resistances are higher, and therefore current transients are slower which should lead to a more balanced behavior). As expected, there is almost no loss difference for T_J = 25°C as the current difference is just as small, but as it increases with temperature, it is also reflected in switching loss distribution slightly.

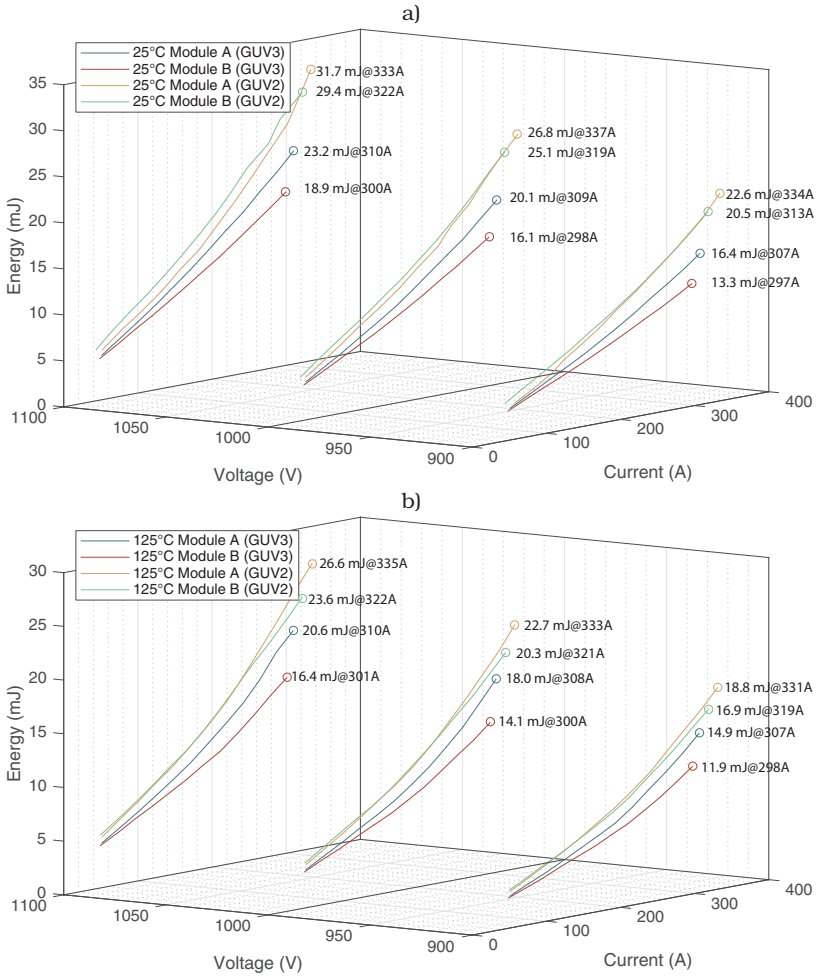


Figure 3.48: MOSFET Turn-on energy loss for modules A and B as a function of I_D per module and V_{DS} for both gate unit tested resistances. a) Energy loss results for T_J = 25°C. b) Energy loss results for T_J = 125°C.

On the other hand, in Fig. 3.49 turn-off switching loss distributions for both gate unit resistance pairs are presented. In this case, it is observable that turn-off energy is almost perfectly distributed among devices. A small difference is observed because of the different driven currents, (this effect is more visible at the end of the curve, because even if the curves are close to overlapping, each pulse present slightly different currents per module) however this difference is very small for all measured datapoints.

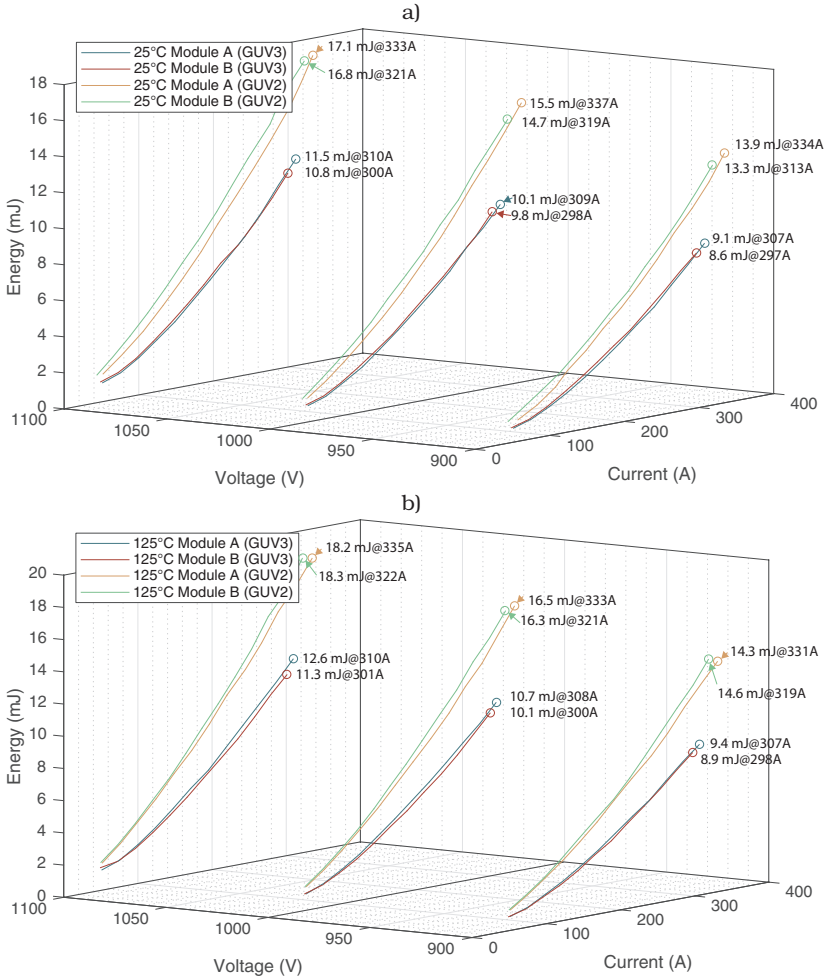


Figure 3.49: MOSFET turn-off energy loss for modules A and B as a function of I_D per module and V_{DS} for both gate unit tested resistances. a) Energy loss results for T_J = 25°C. b) Energy loss results for T_J = 125°C.

Finally, in Fig. 3.50 diode reverse recovery loss distributions for both gate unit resistance pairs are presented. As observed, the behavior of the curves is more erratic in this case, as the signals present more oscillations due to parasitic interactions in the parallel-connected modules and this difficults the determination of the cutoff time to calculate the reverse recovery energy. However, as previously explained, the modules under parallel operation should not drive over 200 A per module, and up to that point the curves present a clear tendency that can be used to create the loss models for parallel-connected modules. Additionally, it should be mentioned that although current distribution among modules is always higher in the Diodes, since this current is product of stored charge in the junction capacitor, higher currents lead to shorter times, hence the loss among devices should not vary much by default.

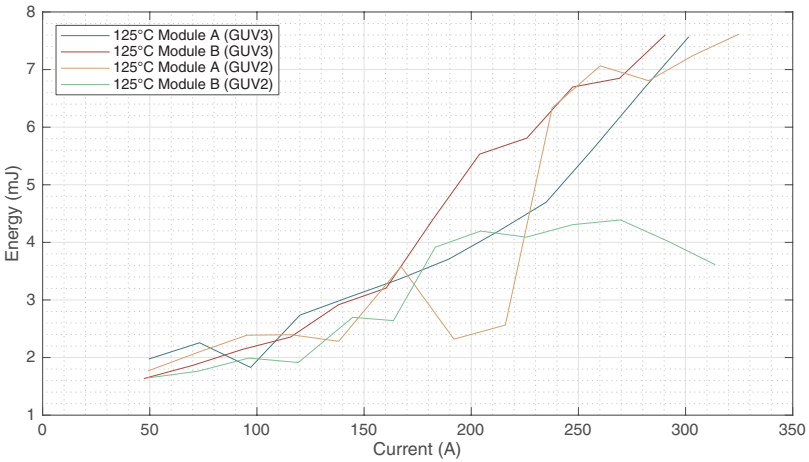


Figure 3.50: Diode Reverse recovery loss as a function of I_F per module and V_F for both gatedriver tested resistances at the critical case scenario: T_J = 125°C and V_{DC} = 1100V.

To summarize the findings, an energy loss graph presenting expected working points using the GUV3 for both modules is presented in Fig. 3.51. As it can be observed from the figure, the total switching loss difference among the modules A and B is very small, being in worst case scenario close to 2 mJ. This should further improve when considering that hotter modules will drive less current due to changes in the $R_{DS(on)}$ resistance.

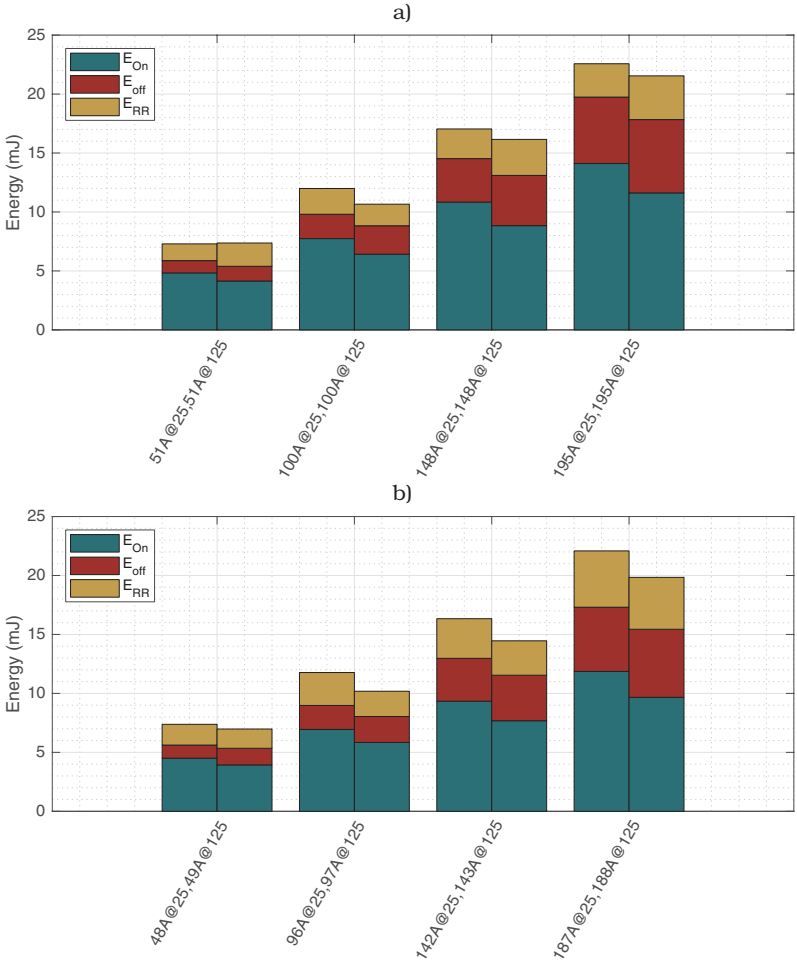


Figure 3.51: Summary of total energy loss per module for the GUV3 gate resistance tested pair for V_{DS} = 1100 V. a) Module A for four different I_D values and for T_J = 25 and 125°C. b) Module B for the same conditions. Left bar represents values at T_j = 25°C, and right bar T_j = 125°C

Transient Signal Data and Timing values

1. Transient Signals:

   In Figs. 3.52 and 3.53, MOSFET turn-on transient/Diode turn-off transient, and MOSFET turn-off transient respectively for a driven current of 400 A at a blocking voltage of 1100 V can be observed. These signals are presented at T_j = 125°C, as they are closer to operating conditions than the T_j= 25°C results.

   Regarding MOSFET turn-on transient in Fig. 3.52. it can be observed that the current present new oscillation modes when compared to the single module switching curves. These oscillations can be attributed to slightly dephased oscillations of similar frequency due to parasitic elements in both modules, which would lead to this oscillation pattern before reaching steady state. However their exact origin has not been tracked as it was not objective of this study. On the other hand, observing the SiC-diode curves, it can be clearly observed that the dv/dt of the diode is the critical among the presented switching curves, as it was for the single device case. Additionally, it can also be observed how now the reverse recovery currents of both diodes, being misaligned and different in magnitude, give as result the mentioned different current oscillations patterns that add complexity to pinpointing the final integration time to determine the reverse recovery energy.

   Finally, regarding turn-off transient signals in Fig. 3.53, it can be observed that they also present the same resonant frequency with similar oscillation patterns. Regarding peak turn-off current, this also occurs at different times, however, the overlap area with V_{DS} is almost the same, which results in similar energy, as it was already described in Fig. 3.49.

2. di/dt and dv/dt

   As previously discussed, di/dt most critical aspect is that it can generate overvoltages during MOSFET turn-off, which could generate avalanche effects if the blocking voltage were to be surpassed. However, from all measurements, the worst case scenario was indeed during MOSFET turn-off, generating app 11 A/ns at 25°C, I_{Dtotal} = 600 A. However, and although this high di/dt generated voltage peaks close to 1600 V, the stray inductance of the converter is to be smaller, as the switching loop among devices is smaller due to the absence of the shunt resistor and the corresponding bends in the DC-Link plates to allocate it. Furthermore, close to 400 A the di/dt is close to 7 A/ns, hence not producing such critical overvoltages.

   Regarding dv/dt, the critical case (as exposed in the transient figures) is the diode dv/dt, and observing Fig. 3.54, the critical case occurs at 125°C with 65 V/ns. This is indeed a high dv/dt value, which although is supported by other SiC semiconductor manufacturer companies, it has not been guaranteed by Rohm, which only expresses that devices have been used up to 50 V/ns without any observed deterring effects. This however does not mean that they cannot be used over 50 V/ns, as this affirmation was not a granted 50 V/ns usage or a limit for this value as maximum. Nonetheless, when considering the 200 A per device mark, the dv/dt values are quite close to 50 V/ns, which is high, but within manufacturer tested limits.

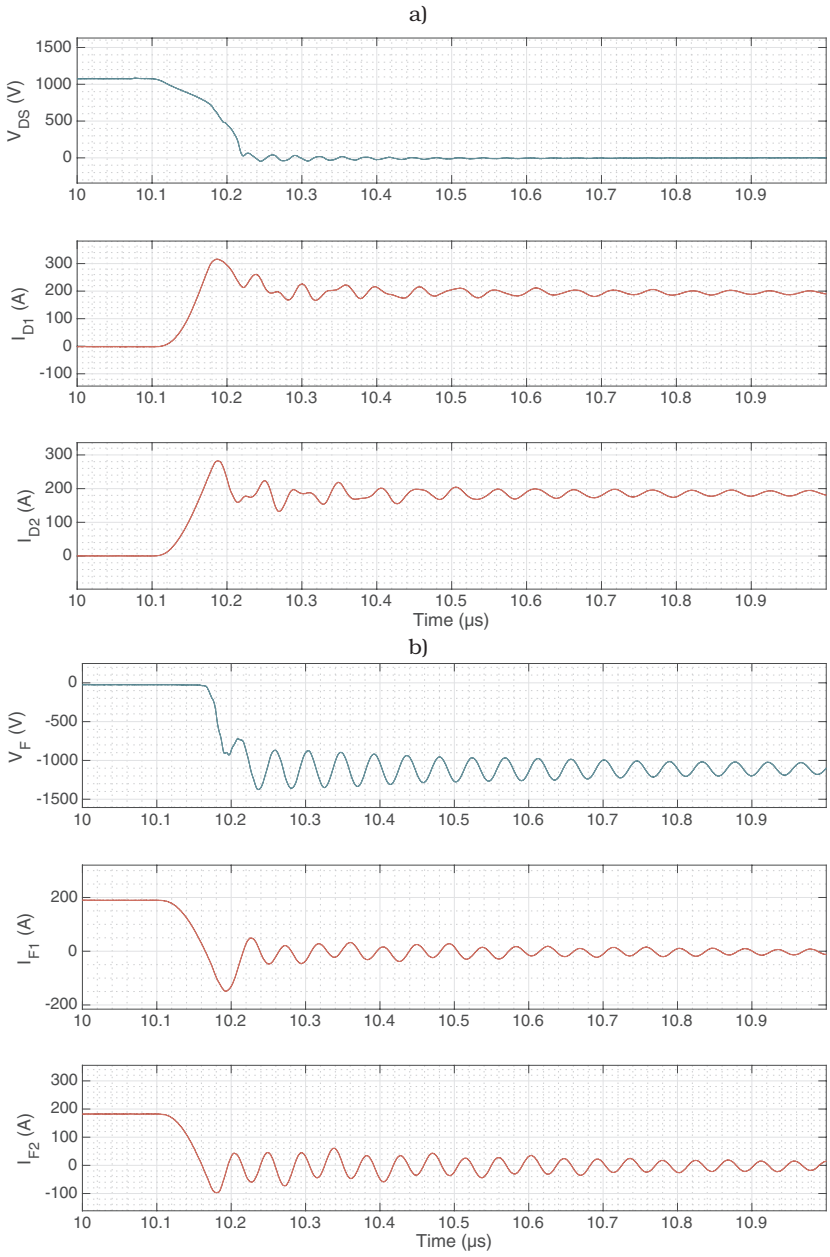


Figure 3.52: SiC-MOSFET turn-on transient and diode turn-off transient signals for I_{Dtotal} = 400 A, $V_{DS/F}$ = 1100 V and T_J = 125°C for GUV3 and $R_{G(on)}$ = 1 Ω. a) MOSFET turn-on transient results. b) Diode turn-off transient results.

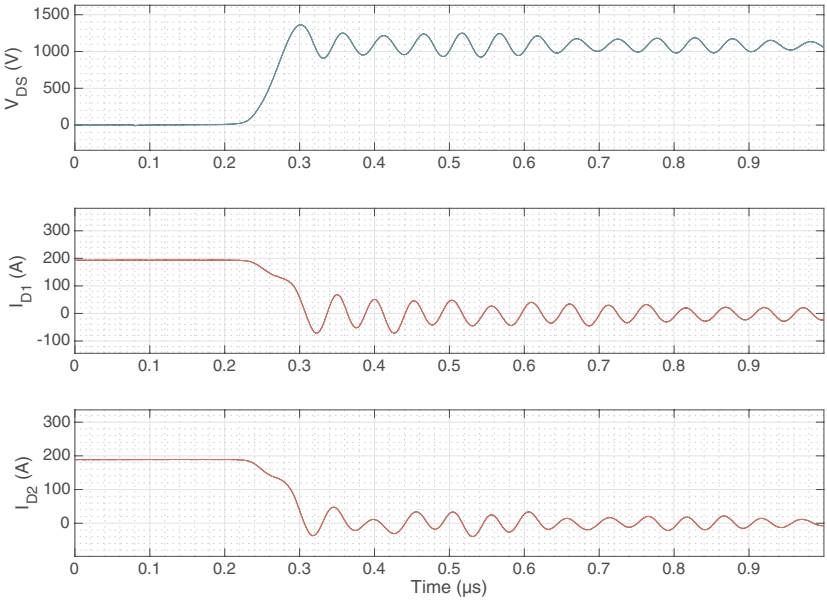


Figure 3.53: SiC-MOSFET turn-off transient for I_{Dtotal} = 400 A, V_{DS} = 1100 V and T_J = 125°C for GUV3 and $R_{G(off)}$ = 0.2 Ω.

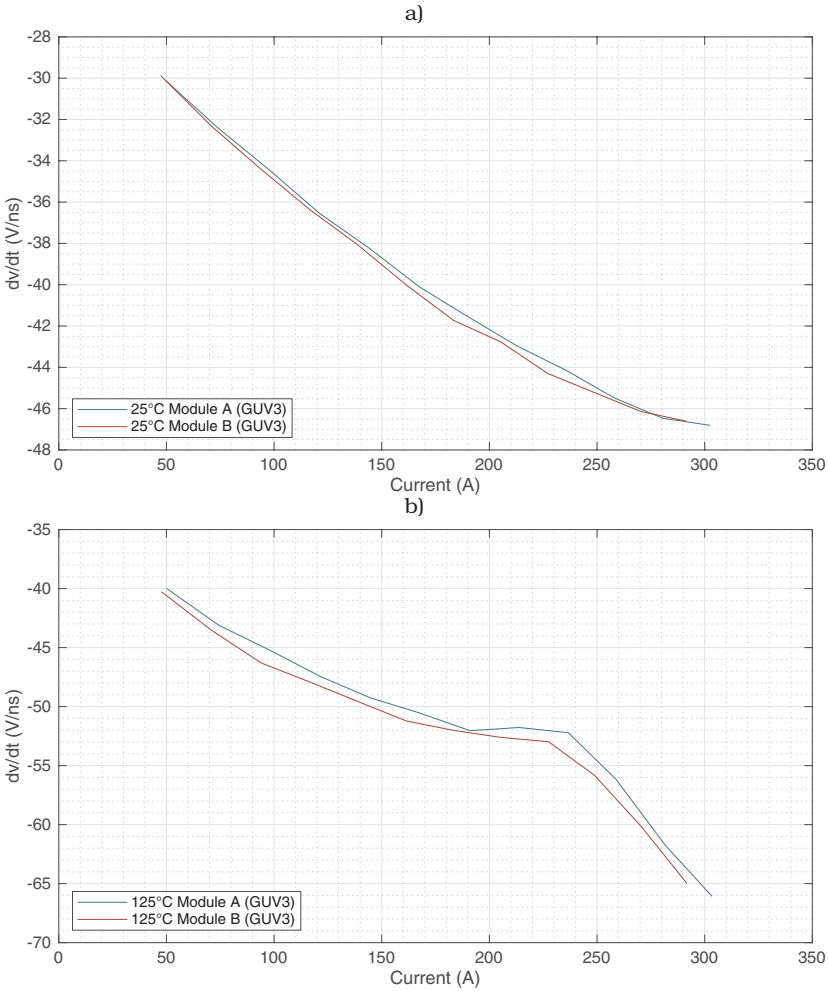


Figure 3.54: Critical dv/dt values for the SiC module vs driven current per module: Diode turn-off dv/dt transient values at a blocking voltage of 1100 V. a) Results at 25°C. b) Results at 125°C.

3. Timing data

   Finally, timing data of the devices using the GUV3 is presented in Figs. 3.55 and 3.56 for turn-on and turn-off respectively. Please note though, that since no gate voltages were measured in the parallel connection of modules, the turn-on/off delay is measured from the turn-on/off signal flank in the controller, and not from the 0.1/0.9 gate voltage value. This leads to a worst case scenario calculation for the delay time, hence being safer for deadtime setting purposes.

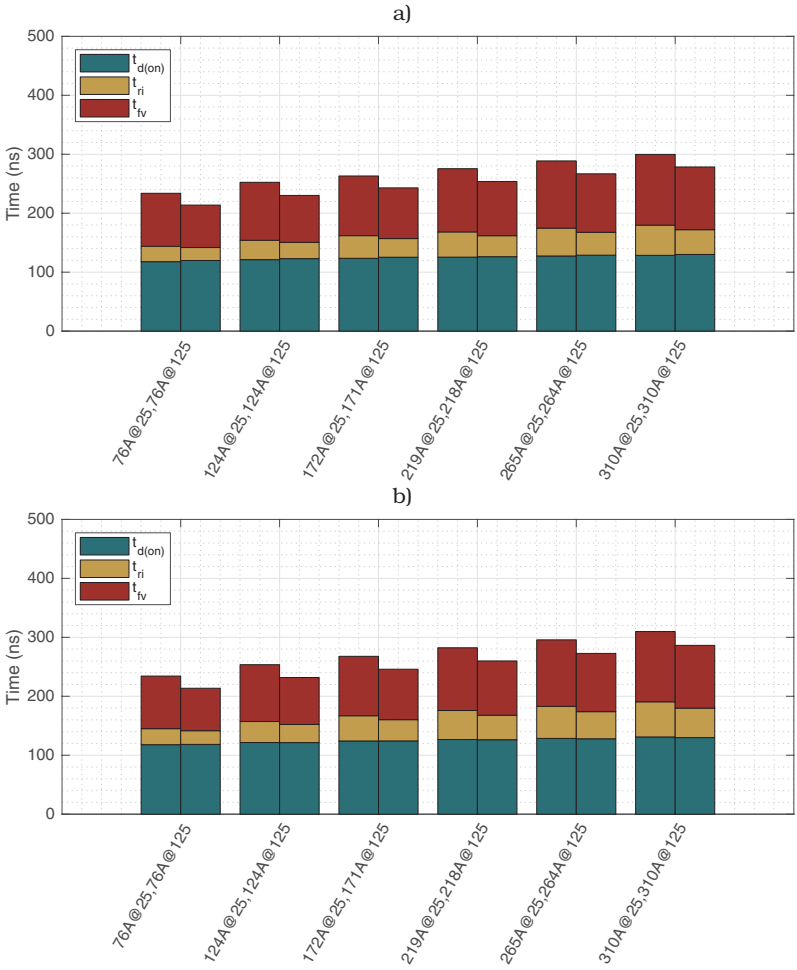


Figure 3.55: Turn-on timing summary for GUV3 driven modules. a) Module A at 25°C and 125°C. b) Module B at 25°C and 125°C.

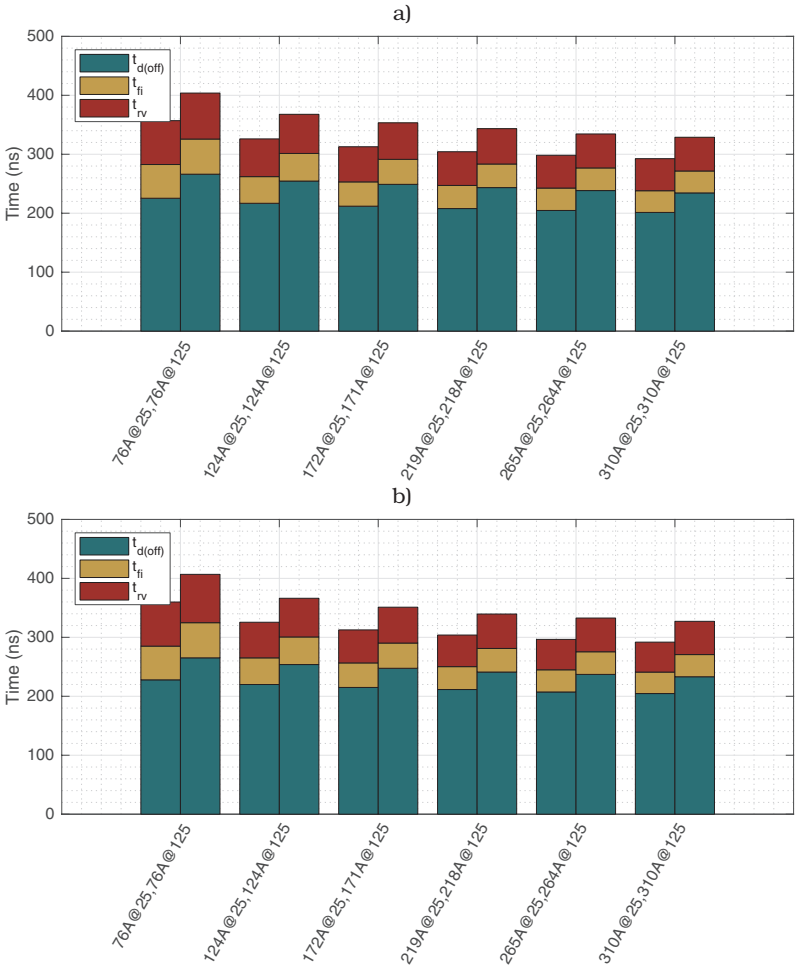


Figure 3.56: Turn-off timing summary for GUV3 driven modules. a) Module A at 25°C and 125°C. b) Module B at 25°C and 125°C.

From the figures, it can be observed that the two modules present very similar, compatible switching times. This of course is to be expected as the devices share the gate unit and kelvin emitters, hence forcing the behavior by design. From the figures, it can be concluded that 500 ns (0.5 μs) is more than enough deadtime to ensure safe operation of the converter.

3.3.4 Parallel-connected Module Results Summary

The parallel-connected constellation of devices has been analyzed through double pulse tests and forward measurements with focus on current and loss sharing. From the obtained results, the main conclusions remain the following:

- Parallel-connected modules present a good driving current symmetry in spite of high switching speed under the tested parallel connection strategy.
- Even with detected current asymmetry, turn-on switching loss differences with the GUV3 do not exceed 4 mJ. And when adding all switching losses, this effect does not surpass 2 mJ. Particularly when running into full load and high temperature, the differences account for 3% of the overall switching losses.
- Current difference during current reverse recovery is the most uneven magnitude in the system, which can be in real-time up to 16.25% of the total driven current at V_{DS} = 1100 V, $R_{G(on)}$ = 1 Ω for the range of operation of the SiC converter demonstrator (400 A).
- Largest measured dv/dt in the system occurs at diode turn-off at T_J = 125°C. Being at the maximum measured current 65 V/ns, and close to 53 V/ns at 200 A per device with $R_{G(on)}$ = 1 Ω.
- Currents flowing through source pins is lower than 5 A in on-state while using the GUV3, hence it can be used safely.
- Hence, the parallel connection of these two SiC-MOSFET modules can be performed while using the recommended Manufacturer's gate resistances in the range of interest of the SiC demonstrator testbench without need for derating in spite of high switching speed.

3.4 Summary

In this chapter, the characterization of the 1700 V, 250 A Half-bridge Full-SiC module BSM250D17P2E004 from Rohm has been characterized both in single and parallel-connected operation. Several comparisons in different operation points, and also against SI-IGBT devices have been performed, concluding that the SiC-MOSFET module presents extended switching frequency capability at a fraction of the Si-IGBT loss (up to aprox. 10 times less switching energy), which can be harvested as long as dv/dt and common mode paths are considered in the design. Finally, successful parallel operation capability of the SiC-MOSFET modules has been confirmed, enabling the construction of the converter demonstrator by using this power block configuration.

4 The SiC Converter Demonstrator

In this chapter, the reader will be introduced to the realization of the SiC converter demonstrator that was built to determine advantages, constraints and challenges that are faced when building a low voltage high power grid connected industrial converter based on SiC semiconductors. First, an overview of the main requirements the converter must comply with is presented. This is then followed by a detailed description of the design steps, to then discuss the final converter construction, its experimental results and the main lessons of the construction process and its commissioning.

4.1 Summary of Converter Requirements and Design Procedure

The main goal of this work has been to determine basic characteristics, advantages and limitations that SiC technology based converter designs for low voltage high power grid connected industrial applications present. And to that end, a SiC based industrial converter demonstrator with grid connection following industrial design criteria has been developed. The converter requirements are the following:

- Topology: Three-phase two level grid-tied inverter

  The converter topology has been defined to be the three-phase two level grid-tied inverter, as this converter topology is the standard for industrial applications [82, 83], while being also reliable and requiring the minimum amount of power switches required to perform in three-phase applications with 4 quadrant power control capability.

- Grid Voltage: 690 V_{ll}

  Since in industrial converters the main driver are material and manufacturing costs, in order to be competitive while using Silicon carbide one of the most important gain factors must be system cost savings. It was observed by the industry partner that the 690 V_{ll} SiC converter is, from this perspective, more attractive than the 400 V_{ll} variant, hence being of particular interest to analyze system gains in this variant, as this should sketch the borders at which SiC-based converter starts becoming an attractive solution for this market.

- Switching frequency: 20 kHz

  The converters switching frequency was a topic of study, but the best compromise was determined to be 20 kHz. The reason of this first assessment rests on several facts, being the most important that switching frequencies around this range allow the usage of laminated silicon steel, which is a cost-effective solution for grid connected inductors. Additionally, although SiC-MOSFETs can switch faster, scaling switching frequency to 40

or 60 kHz will not help to observe efficiency improvements, while at the same time the additional loss will reduce nominal current as the cooling system was defined by the industry partner. Moreover, a switching frequency of 20 kHz is over human hearing frequency range, while presenting important filter size reductions in both weight and volume, enabling the use of cost-effective core materials as well.

- Nominal DC-Link voltage: 1080 V

  The nominal converter DC-Link voltage was determined to be 1080 V. This was defined as a design requirement because of control related reasons. The converter generated voltage vectors in the $\alpha\beta$ space must always be able of generating higher voltages than the grid voltage V_S plus the voltage drop in the filter V_{filter} in order to control the power at all times. Since the critical value for the generated converter voltages is exactly halfway between two vectors, this leads to:

$$\left| \frac{V_{DC(min)}}{\sqrt{3}} \right| \geq |V_S + V_{filter}| \tag{4.1}$$

  from which, neglecting the filter voltage drop, which is small by design, the minimum DC-Link voltage value for a 690 V_{ll} grid is 975 V. However, this value is only to break even, and therefore a 10% increase has been included, hence V_{DC} = 1080 V. This and along the extra 15% the usage of 3rd harmonic injection provides warranties that the space vectors of the converter will be enough to control power flow at all times.

- Nominal Power: 230-300 kVA

  In order to be comparable with silicon-based industrial converter alternatives for 690 V_{ll}, the converter should provide a nominal power in the range 230-300 kVA. This was an industry partner defined goal. Its implications are that the approximated load current should belong to the [193-251] A_{RMS} range ([272-355] A_{Peak}), which due to module current capability options at the beginning of the project required module parallel connection in order to be achieved.

- Converter must be rated according to different load profiles required by industrial inverters while each module's die average junction temperatures $T_j \leq 125°C$ at all times.

  Industrial inverters should be able to operate under different load conditions, as these are not constant in these environments, and defining the nominal current by applying the maximum load results in a higher nominal current than the one the converter would present if it is subjected to overload scenarios. Hence, in order to properly rate the converter, the nominal current must be determined by ensuring that the defined load conditions do not overheat the corresponding module die junctions, and therefore one of the main requirements is to ensure that the average junction temperatures of the devices within the module are less or equal to 125°C for all allowed load profiles, even if is not planned that the demonstrator operates under load profile tests.

- Ambient temperature: 45°C

  The considered maximum ambient temperature for all calculations in this

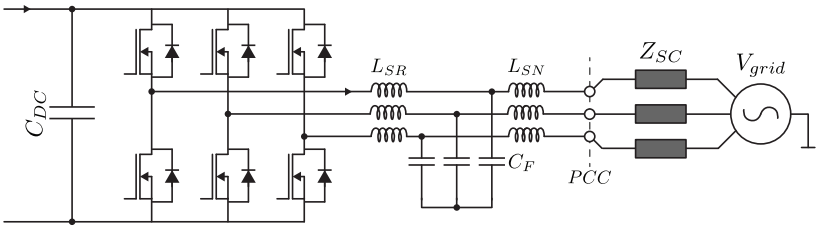


Figure 4.1: Converter schematic of the grid-tied 3Ph-2L VSI with LCL-Filter.

work is 45°C because up to 40°C, typical industrial converters are ensured to be operation capable without any need for de-rating. Consequently, 45°C is a good ambient temperature to determine the converter nominal characteristics.

- IEC/TS 62578 and EN61000-2-2 grid-code harmonic emission are to be considered for compliance by means of using an LCL-Filter with active damping control algorithms

  In converters of this category, LCL-Filters are an attractive, state of art solution for complying with grid-codes. As an agreement with the industry partner, both the IEC/TS 62578 and the EN61000-2-2 norms were considered for filter design, being the IEC/TS 62578 a hard requirement requested from the industry partner, and the EN61000-2-2 a soft goal, (or guideline) proposed by the TU-Dresden. Additionally, active damping control solutions to deal with the LCL resonant frequency have been requested, as passive solutions would hurt efficiency, which is one of the secondary figures of merit this work is interested in.

- Rack and cooling:

  The converter must be built in a defined rack, which was provided by the industry partner and was agreed on both parts to be used. The overall volume is 48.65 x 27.85 x 110.6 cm^3, and this includes the cooling solution, which is a Heatsink with forced cooling provided by the fan on the bottom of the rack (see Fig. 4.16)

- Control method: Voltage oriented control with Space Vector Modulation (SVM) and active damping.

Therefore, due to the conditions and requirements defined to build the power converter, the procedure was determined as follows: First, the converter nominal current needs to be determined, as it is an important input parameter for the design of several important components of the converter. Once the nominal current is defined, DC-Link design and construction are discussed, to finally present the main filter design characteristics. It is important to remark though, that only the general facts of filter design will be discussed, as this topic is part of another ongoing PhD. dissertation on the TU-Dresden chair of power electronics. Finally, the converter implementation and main experimental results confirming the design goals are presented. A diagram of the converter topology with the corresponding LCL-Filter can be found in Fig. 4.1.

4.2 Determination of the Nominal Phase Current I_N

The converter must be properly rated in order to determine the maximum current capability of the converter while complying with several load case scenarios. This is of importance not necessarily because it is an objective of the prototype to operate under different load profiles, but to properly rate it to be adequately comparable with existing available converters, as a converter that advertises a determined nominal current and is capable of operating under different load profiles, would be capable of a higher nominal current by providing power to a steady load.

As previously explained, the nominal current of the converter needs to comply with these different load scenarios while keeping junction temperatures under 125°C and an ambient temperature of 45°C. To that end, loss simulation coupled with thermal models are necessary in order to determine the converter nominal current.

The corresponding load profiles that the converter needs to be able to perform are presented in Fig. 4.2. and the corresponding scenario defining values are presented in Table. 4.1.

Table 4.1: Load profile scenario parameters.

		Current	Time
Scenario 1	Steady load	$I_{LO} = 0.93\ I_N$	240 s
	Overload	$I_{ov} = 1.1\ I_{LO}$	60 s
	Total Period		300 s
Scenario 2	Steady load	$I_H = 0.83\ I_N$	240 s
	Overload	$I_{ov} = 1.5\ I_H$	60 s
	Total Period		300 s
Scenario 3	Steady load	$I_{S6} = 0.7\ I_N$	54 s
	Overload	$I_{ov} = 2\ I_{S6}$	6 s
	Total Period		60 s

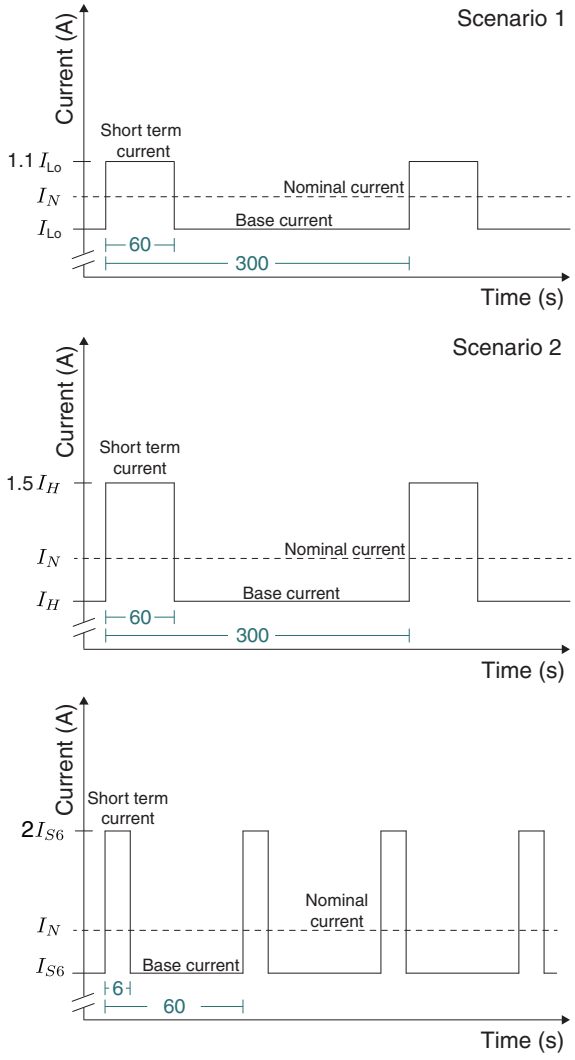


Figure 4.2: Load profile scenarios. Scenario 1: Light overload profile. Scenario 2: Strong overload profile. Scenario 3: S6 overload profile.

Therefore, in order to determine the nominal current of the converter, calculations/simulations to estimate module loss must be performed. Then, the resulting data is coupled with thermal models in order to calculate the junction temperature of all internal dies and maintain them below 125°C in the worst case scenario. To that end, analytical calculations of converter loss were performed to then verify the validity of the simulation scheme. Once this was performed, a three step simulation strategy was developed, in order to determine the maximum nominal current that complies with max. junction temperatures and load profile requirements.

4.2.1 Fundamentals of Converter Loss Calculations

The classical approach for converter loss calculations presented for example in [84], where loss estimations are presented for an IGBT based three phase two level inverter with SPWM modulation for both conduction and switching losses. However, typically the presented analytical results do not include 3rd harmonic injection and do not consider MOSFET characteristics, as these devices were not widely used for inverter applications before Silicon Carbide, which is why this topic will be shortly discussed here.

- Conduction Loss

  For conduction loss calculations, the main idea can be traced back to [85], in which the main objective is to define the energy loss during conduction as a function of the duty-cycle, the dephase angle between current and voltage φ, and the modulation index M. The modulating signal is introduced as means of calculating the duty-cycle, which in turn defines if switch or diode conduct at any given time. Thus, the energy is result of forward voltage, times the current magnitude flowing at the time, times the dutycycle. This can then be integrated if the duty-cycle is considered a differential of time for practical purposes, in half a cycle and divided through the period to get the average conduction loss. This can be observed for the MOSFET in first quadrant as

$$P(W) = \frac{1}{T}\int_0^{T/2} \hat{I}_L \sin(\omega t)\cdot\hat{I}_L \sin(\omega t) R_{DS(on)}\cdot\left(1 + M\left(\sin(\omega t + \varphi) + \frac{\sin(3(\omega t + \varphi))}{6}\right)\right) dt \tag{4.2}$$

  in which the current at any given time is given in red, the forward voltage is described in yellow, and the modulating signal with third harmonic injection is described in dark green. Please note that in this case, the modulation index is defined as $0 \leq M \leq 2/\sqrt{3}$ and not as $0 \leq M \leq 1$, which is how it is defined in [85]. The result for the MOSFET conduction loss in first quadrant is presented in (4.3). The same analysis can be done for the Diode while the channel is not conducting, which leads to (4.4).

  Regarding these calculations though, there is an important difference when comparing IGBT and MOSFET based converters conduction loss calculations. Since IGBTs conduct in only one direction, either the IGBT or the diode are conducting at a determined time. Hence, there are no current sharing considerations that need to be included in the model. This is not the case when using MOSFETs, because in this case there is the option

to perform active rectification, which consists in turning on the MOSFET while the diode is conducting to use the MOSFET channel to drive current as well. This occurs automatically through classic modulation of the leg, as turning off a device means turning on the complimentary, regardless of current direction flow. This means that when modulating a positive voltage with negative current, the switch next to the driving diode is automatically turned on. In this work, the first approach to this problem was to use the datasheet voltage drop of the active rectification curve and approximate it through a 3rd order polynomial that crossed through zero. This polynomial expression was in turn then used for loss calculations following the same presented procedure as for the first quadrant. Afterwards, using the corresponding Diode voltage drop that was obtained by using this expression, the diode forward current is expressed. Then, forward voltage drop is calculated by using the diode defined current, and hence with it diode loss is calculated. Finally, MOSFET loss was calculated as the difference between the active rectification loss (fitted curve) and the diode loss. However, and as functional as this solution is, it is not an elegant solution, which is why afterwards a more general solution was described based on the resistive behavior of the channel and the diode characteristic, leading to the result presented here.

In this case, since the devices are in parallel, the forward drop voltages can be used to calculate the current difference among devices ($V_{f0} + R_d I_f(t) = R_{DS(on)} I_D(t)$). Since the load current is the sum of the diode current and the MOSFET current ($I_L(t) = I_D(t) + I_f(t)$), the current expressions for both MOSFET and diode can be expressed in function of the device parameters and the load current. Thus the loss calculations can proceed exactly as calculated for the diode, by only considering the new expressions of current to write the energy expression. The shared current conduction loss expressions for both the MOSFET and the diode can be found in (4.5) and (4.6) respectively.

First Quadrant

- MOSFET conduction loss:

$$P_{cond_{MOS}} = \frac{\hat{I_L}^2 M R_{DS(on)} \cos(\varphi)}{3\pi} - \frac{\hat{I_L}^2 M R_{DS(on)} \cos(3\varphi)}{90\pi} + \frac{\hat{I_L}^2 R_{DS(on)}}{8} \quad (4.3)$$

Third Quadrant

- Diode loss while MOSFET channel is off:

$$P_{cond_{diode}} = \hat{I_L}^2 R_d \left(\frac{1}{8} - \frac{M\cos(\varphi)}{3\pi} + \frac{M\cos(3\varphi)}{90\pi} \right) + \hat{I_L} V_{f0} \left(\frac{1}{2\pi} - \frac{M\cos(\varphi)}{8} \right) \quad (4.4)$$

- Loss during active rectification mode:

$$P_{cond_{MOS}} = \frac{\hat{I_L}^2 M R_d^2 R_{DS(on)} \cos(3\varphi)}{90\pi(R_d + R_{DS(on)})^2} - \frac{\hat{I_L}^2 M R_d^2 R_{DS(on)} \cos(\varphi)}{3\pi(R_d + R_{DS(on)})^2} + \frac{\hat{I_L}^2 R_d^2 R_{DS(on)}}{8(R_d + R_{DS(on)})^2} - \frac{\hat{I_L} M R_d R_{DS(on)} V_{f0} \cos(\varphi)}{4(R_d + R_{DS(on)})^2} + \frac{\hat{I_L} R_d R_{DS(on)} V_{f0}}{\pi(R_d + R_{DS(on)})^2} - \frac{M R_{DS(on)} V_{f0}^2 \cos(\varphi)}{2\pi(R_d + R_{DS(on)})^2} - \frac{M R_{DS(on)} V_{f0}^2 \cos(3\varphi)}{36\pi(R_d + R_{DS(on)})^2} + \frac{R_{DS(on)} V_{f0}^2}{4(R_d + R_{DS(on)})^2} \tag{4.5}$$

$$P_{cond_{diode}} = \frac{\hat{I_L}^2 M R_d R_{DS(on)}^2 \cos(3\varphi)}{90\pi(R_d + R_{DS(on)})^2} - \frac{\hat{I_L}^2 M R_d R_{DS(on)}^2 \cos(\varphi)}{3\pi(R_d + R_{DS(on)})^2} + \frac{\hat{I_L}^2 R_d R_{DS(on)}^2}{8(R_d + R_{DS(on)})^2} - \frac{\hat{I_L} M R_{DS(on)}^2 V_{f0} \cos(\varphi)}{8(R_d + R_{DS(on)})^2} + \frac{\hat{I_L} M R_d R_{DS(on)} V_{f0} \cos(\varphi)}{8(R_d + R_{DS(on)})^2} + \frac{\hat{I_L} R_{DS(on)}^2 V_{f0}}{2\pi(R_d + R_{DS(on)})^2} - \frac{\hat{I_L} R_d R_{DS(on)} V_{f0}}{2\pi(R_d + R_{DS(on)})^2} + \frac{M R_{DS(on)} V_{f0}^2 \cos(\varphi)}{2\pi(R_d + R_{DS(on)})^2} + \frac{M R_{DS(on)} V_{f0}^2 \cos(3\varphi)}{36\pi(R_d + R_{DS(on)})^2} - \frac{R_{DS(on)} V_{f0}^2}{4(R_d + R_{DS(on)})^2} \tag{4.6}$$

The main limitation of this approximation model is that the diode data is usually measured for just a handful of temperatures. Hence, since forward characteristics are temperature dependent, 3rd quadrant loss estimations while current sharing occurs is more subject to error if the junction temperature of the devices does not match the temperature at which the parameters were extracted from the datasheet. This is especially important when considering active rectification calculations, as small variations in the device forward voltages can influence current distribution and hence incur in loss estimation errors.

- Switching Loss

  Switching loss equations are straightforward to use, as there is absolutely no change from the typically used IGBT three-phase two level inverter when compared with a MOSFET based variant. They can be found in [84], and are written here for completitude. The MOSFET loss can be calculated as

$$P_{sw_{MOS}} = f_{sw}(E_{on} + E_{off}) \frac{\hat{I_L}}{I_{ref}\pi} \left(\frac{V_{CC}}{V_{ref}}\right)^{K_v} (1 + Tc_{E_{sw}}(T_J - T_{ref})) \tag{4.7}$$

  where $E_{on/off}$ are the corresponding energy losses, I_{ref}, V_{ref} and T_{ref} are the current/voltage/temperature at which the energy losses were registered respectively, K_v is an exponent to adjust the dependency of voltage and switching loss and $T_C E_{sw}$ is the thermal coefficient, which is to be included if the loss calculations are performed too far from the reference temperature.

  On the other hand, the diode switching loss calculations can be performed

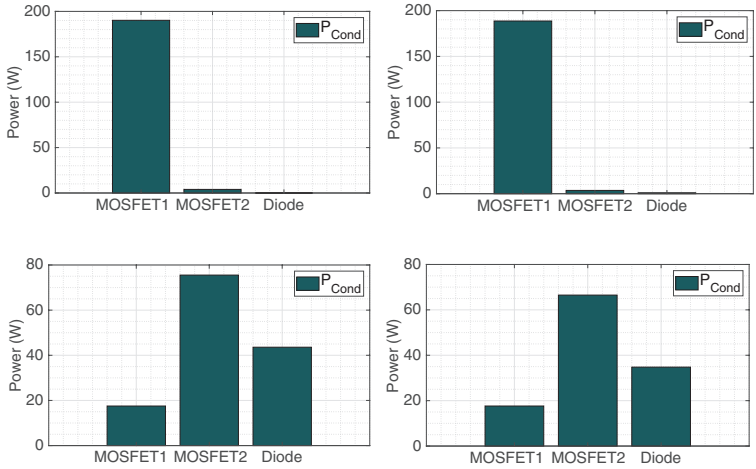


Figure 4.3: Comparison of conduction loss by theoretical equations and simulation results for $R_{G(on)} = 0.8\,\Omega$, $R_{G(off)} = 0.6\,\Omega$, $I_L = 250\,A$, $V_{DC} = 1080\,V$. Left and right: Theory based and simulation based conduction loss results respectively. Up and Down: $M = 2/\sqrt{3}$, $\cos(\varphi) = 1$ and $M = 1$, $\cos(\varphi) = -1$ respectively.

by using

$$P_{sw_{Diode}} = f_{sw}(E_{RR})\frac{\sqrt{2}}{\pi}\left(\frac{\hat{I_L}}{I_{ref}}\right)^{K_i}\left(\frac{V_{CC}}{V_{ref}}\right)^{K_v}(1 + Tc_{E_{sw}}(T_J - T_{ref})) \tag{4.8}$$

where E_{RR} is the measured reverse recovery loss and K_i is an exponent to adjust the dependency of driven current and switching loss.

Conduction and switching loss expressions were then used by extracting datasheet parameters (conduction loss), recommended coefficient values and experimental switching energy losses to then compare its results with the simulation scheme that was built to evaluate the load scenario profiles in order to verify and validate simulation results. These simulations are based in PLECS, and modulates the switches to then calculate loss by using the obtained data from the characterization experiments. Comparison results can be found in figs 4.3 and 4.4 for the conduction and switching loss comparisons respectively.

Through these comparisons, it was possible to observe that the simulation model presents similar loss, typically being the theoretical variant a slightly worst-case scenario than the simulated case. This is attributed in switching losses to the temperature swing during a cycle that the theoretical model cannot modelate. On the other hand the most noticeable difference presents itself in conduction loss 3rd quadrant behavior, however this is also attributed to the high dependency of the parameters and its corresponding current sharing behavior to tem-

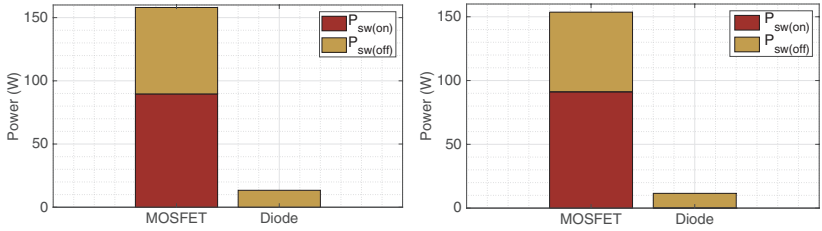


Figure 4.4: Comparison of switching loss by theoretical equations and simulation results for $R_{G(on)}$ = 0.8Ω, $R_{G(off)}$ = 0.6 Ω, I_L = 250 A, V_{DC} = 1080 V, f_{sw} = 20 kHz. Left and right: Theory based and simulation based switching loss results respectively.

perature. However, the overall loss distribution of the theoretical models is well reflected by simulations, and hence it was considered a valid model to determine the nominal current of the converter.

4.2.2 Thermal Modeling

Once the loss model simulation scheme was established, it is necessary to use an adequate thermal model to be able to traduce the obtained loss into junction temperature values. The cooling system model to be used in this work was previously agreed with the industry partner, and it corresponds to a thermal model for single module devices based on the econodual package format that was used in a previous generation of converters of the same line that this rack belongs to. This is not the rack that was finally used to build the converter, but it is the model with which all components were designed. Hence, it will be presented here.

In general, to develop thermal models the state of art solution today is to use thermal impedance curves [17, 18]. A thermal impedance curve is calculated from the cooling stage of a system, and equals to the delta temperature of the path (junction to case, junction to ambient, etc.) divided by the loss. In other words, it represents the temperature delta that an applied constant power generates on the device. These curves allow to calculate temperature development during thermal transients, which is exactly what is necessary to study different load profiles. These transient thermal impedance curves are translated into electronic elements to simulate temperature evolution as if they were electrical magnitudes, because there is an equivalence of thermal an electrical equations. However, it must be kept in mind that these models are an approximation, as always when going from a three dimensional model to a one dimensional one errors are bound to exist. However, these approximations are considered good enough for estimation purposes. For a more precise calculation, strategies such as electro-thermal finite element analysis must be performed.

To obtain the transient thermal impedance of a device, one can refer to [17]. In summary, first a calibration round is measured, in which all devices are heated up over the interesting temperature measuring points by driving current through the modules. Once the devices are hot, the system is turned off and a very small

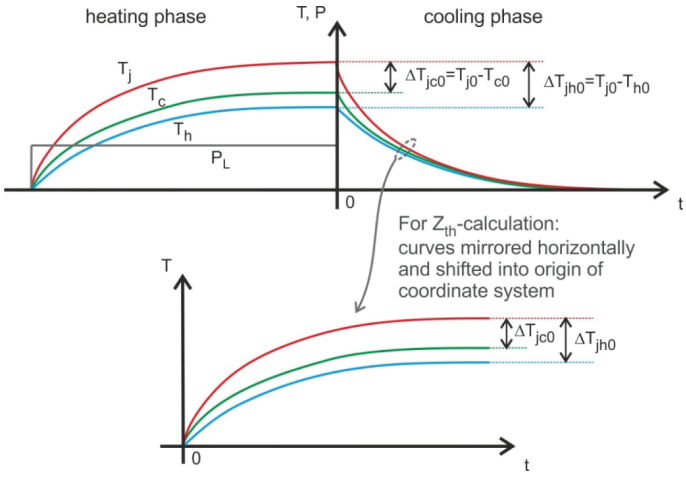


Figure 4.5: Example of a Transient thermal impedance curve. Source: Infineon [17].

current (mA range, equivalent to app. 1/1000 times the nominal current of the module) is driven to generate a voltage drop. At these currents, the voltage drop (V_{CE}, V_F) and the temperature present a linear dependence, and assuming that all devices cool down very slowly (a heatsink with high thermal capacity is required for this to work) the junction temperature can be assumed to be equal to the heatsink temperature after the corresponding module thermal time constants, and then this temperature can be related the corresponding voltage drop. Once the voltage drop and the junction temperatures have been characterized, the system is heated up again with a determined power, to then cool the system down with active cooling. Then curves during this cooling phase can be registered, and junction temperatures can be calculated through voltage drop while driving this small current to be able to calculate thermal impedance curves. These curves are only a reflection of the cooling phase with the x-axis, that are then shifted to the origin [17] (see Fig.4.5)

Foster and Cauer Models

Once these curves are obtained, they need to be transformed to an equivalent thermal circuit that can model temperature dynamic effects. These thermal models are the Foster and Cauer models, and are presented in Fig. 4.6. Both thermal approximations are equally valid, and can represent the same thermal curve. However, both thermal models have their own advantages and disadvantages.

The Foster model, also known as chain model, is the simplest model, and it is preferred for curve impedance extraction because it is easy to approximate from thermal impedance curves, as it corresponds to a sum of exponentials that added represent the curve (partial fractions). To obtain it, a fitting of the sum of

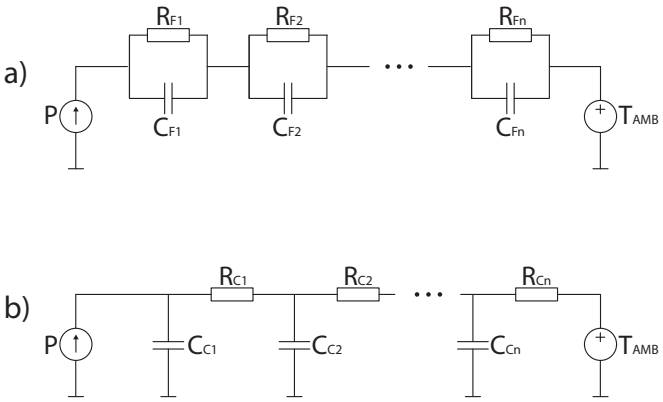


Figure 4.6: Electric models for dynamic thermal calculations. a) Foster model, b) Cauer model.

three to five exponential (typically three are enough) must be performed over the Z_{th} curve to accurately approximate the curve (see Fig.4.7). Its disadvantages are that its nodes do not represent any physical magnitude. Furthermore, these models cannot be chained in series to obtain the total thermal impedance path, as they do not model the delay of heat flow from one node to the next. Therefore they can model the curve they were fitted to, but when connected in series with another Foster chain, the total should not represent the connection.

On the other hand, the Cauer model, also known as the ladder model, is regarded as a physical model, as ideally both its capacitances and thermal resistances could and should be determined from physical parameters. This means that the voltage in every node now can represent the temperature on a physical position in the system (1D model). Furthermore, these models can be chained in series or connected in parallel to represent the total thermal impedance path.

As explained before, both methods can represent the same curves, and therefore there is a mathematical relationship between them. This relationship can be found in [86]. However, simulation software typically performs these transformations automatically, as only Cauer models can be interconnected without incurring in additional error, but Foster models are the ones that are either provided in datasheets, or are most easily fitted from transient thermal impedance curves. This of course implicates that the transformation from the foster model does not have a physical interpretation in the cauer model with the exception of the terminal to terminal expression, but will allow interconnection of models correctly.

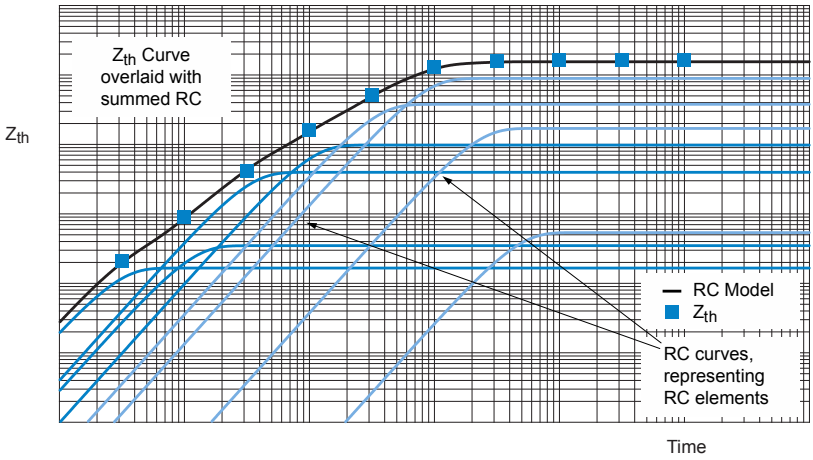


Figure 4.7: Z_{th} curve and added exponential curves to approximate its behavior. Source: NEXPERIA [18].

Table 4.2: MOSFET Foster model parameters.

Term	$R_{th,i}$	$C_{th,i}$	τ_i
1st	0.007 K/W	4.995 Ws/K	3.2 ms
2nd	0.016 K/W	0.019 Ws/K	0.25 ms
3rd	0.063 K/W	0.125 Ws/K	7.9 ms

Module Transient Thermal Model

Due to the fact that the datasheet already provided a thermal impedance curve (see Fig.4.8), this curve has been used for transient thermal analysis. A Foster model has been fitted to this curve, with 3, 4 and 5 stages, determining that 3 stages were more than enough to represent the corresponding curve. The Foster parameters for the three stages can be found in Tables 4.2 and 4.3, for the MOSFET and the diode respectively.

Table 4.3: Diode Foster model parameters.

Term	$R_{th,i}$	$C_{th,i}$	τ_i
1st	0.086 K/W	0.091 Ws/K	7.8 ms
2nd	0.019 K/W	0.014 Ws/K	0.25 ms
3rd	0.009 K/W	3.522 Ws/K	32 ms

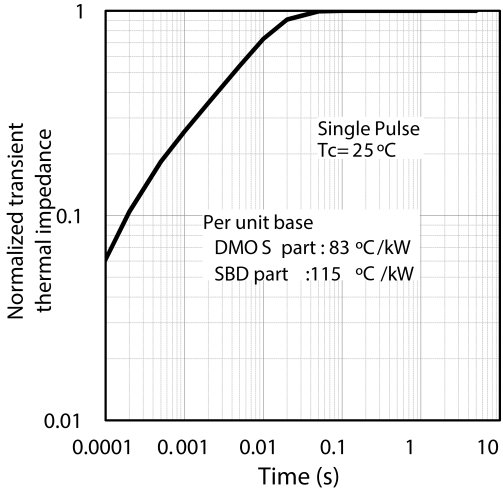


Figure 4.8: Transient thermal impedance curve of the Rohm SiC-MOSFET module. Source: [15].

Heatsink Transient Thermal Model

The heatsink thermal model that has been used for the design is presented in Table 4.4. As mentioned before, since parallel connection of modules are expected to reach the power levels this converter requires, six modules are necessary to do so, two per leg in parallel operation. Hence, in order to make the simulation less compute power taxing, this thermal model has also been scaled to be modeled with a single module (the equivalent model viewed from the terminals of one of the six modules that are mounted over the heatsink) to be able to simulate the temperature rise by simulating only one module instead of all six. This has been done by scaling the heatsink thermal resistances by six and dividing the thermal capacitances accordingly, so the time constants for the equivalent RC stage remain the same. This must be performed this way as time constants are inherent to the system homogeneous response and hence do not change by a change to the inputs of the system (dissipated power). This equivalent model can be found in Table 4.5.

Table 4.4: Provided thermal model of the heatsink.

Term	$R_{th,i}$	$C_{th,i}$	τ_i
1st	0.0056 K/W	2417.97 Ws/K	13.6 s
2nd	0.0064 K/W	185.05 Ws/K	1.2 s
3rd	0.0173 K/W	4082.49 Ws/K	70.4 s

Table 4.5: Equivalent thermal model for simulation purposes from the perspective of a single module of the heatsink with 6 modules configuration.

Term	$R_{th,i}$	$C_{th,i}$	τ_i
1st	0.0336 K/W	404.8 Ws/K	13.6 s
2nd	0.0384 K/W	31.3 Ws/K	1.2 s
3rd	0.1038 K/W	678.2 Ws/K	70.4 s

4.2.3 Nominal Current Determination

Finally, both a validated loss simulation model and the corresponding device thermal models were obtained. Hence the simulation to determine the maximum nominal current was to be performed, and its scheme is presented in Fig. 4.9.

Then, a batch simulation of different currents is performed in a loop until a nominal current for the worst case scenario of the overall load profiles for every tested frequency is determined. However, without optimizations this is a very unefficient method to simulate the system, because:

- Long simulations with small time steps are necessary for a fully modulated thermal simulation of the module (T_{step} 1 µs, while T_{stop} 900 – 1200 s). This is a direct consequence of the time step required to have a reasonable amount of points between switching events using switching frequencies ranging 15-25 kHz, while at the same time the heatsink time constants and the duration of the load profiles require a couple of cycles to reach $T_J \sim 125°C$.
- An estimation of straightforward use of simulation loops would take without simplifications and fixed step between 6 and 40 days to compute in a normal desktop computer, depending on starting point and current steps. As each simulation can range between 45 minutes and 2 hours per current tested due to the fact that the switching frequency defines the simulation step.

Hence, a different strategy was developed to determine the nominal current. This method includes different simulation steps that are clarified in the Fig. 4.10.

The core idea of this simplification scheme is that the model needs only absolute precision at 125°C, as the loops will iterate different currents until any junction temperature crosses the 125°C mark. Hence, if the loss is related to the nominal current for every frequency at 125°C, then no modulation is necessary to perform the simulations and hence the nominal current can be quickly determined.

Each stage performs the following tasks:

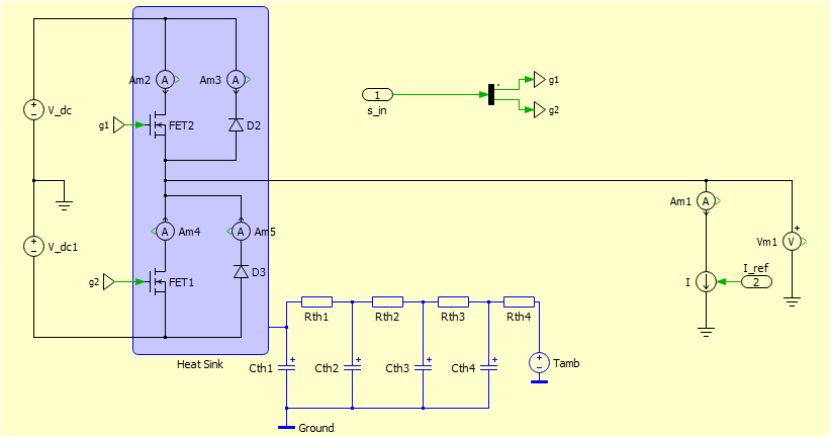


Figure 4.9: Implementation of the loss simulation scheme in PLECS.

- Simulation 1: In this simulation the thermal model of the heatsink is replaced by a voltage source, to directly affect the temperature of the case. This temperature is then varied in nested loops to achieve T_J = 125°C on the corresponding critical junction (which by previous analysis, resulted on the MOSFET always being the critical element). Here, losses, switching frequency, driven current, modulation index and power factor (cos(φ)) are stored, to build a look-up table that evaluates the losses generated by a load current that produce T_J = 125°C in the critical junction. In other words, the following variables are created:
  - $P_M(I_L, f_{sw}, \cos(\varphi), M)@T_{JMavg}$ = 125°C,
  - $P_D(I_L, f_{sw}, \cos(\varphi), M)@T_{JMavg}$ = 125°C,
  - $T_{JMmax}(I_L, f_{sw}, \cos(\varphi), M)@T_{JMavg}$ = 125°C, and
  - $T_{JDmax}(I_L, f_{sw}, \cos(\varphi), M)@T_{JMavg}$ = 125°C,

  where, T_{JXmax} is the maximum junction temperature of the element X(X=M is MOSFET, X=D is Diode), T_{JMavg} is the average junction temperature of the MOSFET (note that the T_{JDavg} is not used, as everything is registered at the junction temperature of the critical element, which was in all cases the MOSFET in this particular study), and P_X is the losses of the device X(X=M is MOSFET, X=D is Diode) as a function of the corresponding parameters and at the temperature of the critical element: T_{JMavg} = 125°C. T_{JXmax} was also captured, which, although not as reliable, due to data extrapolation, served as a first approximation of the ballpark of the maximum junction temperature of a device.
- Simulation 2: In this simulation, the load scenarios are used to apply current amplitudes to the lookup tables that were built in the previous simulation as input to define the loss of each device. This way, all thermal dynamics of the module are eliminated, and only the corresponding R_{th} of each corresponding module is used. On the other hand, the full Cauer

model of the case to ambient path is used (heatsink), and therefore since there is no modulation the simulation speed is drastically improved. Currents are tested in a loop from high currents to low currents until a current that complies with all junction temperatures below 125°C is found. At this current, since is close to T_J = 125°C, its results present high accuracy as the simulations in stage 1 were performed exactly at this point. The output of the test is a proposal of the nominal current for each load profile scenario, depending on switching frequency, cos(φ) and modulation index.

- Simulation 3: Finally, for every frequency, the highest current that complies with all scenarios is simulated in the validation model (full simulation, with all thermal models, with duration several times larger that the heatsink thermal constant and a simulation step in the microsecond range). Since the simulation decoupling (stage 1 and 2) and the resulting approximations are not perfect, the predicted current has been observed to generate junction temperatures that can present an error up to 5 degrees in the simulated events. To correct this, the resulting current has been then be re-simulated in the validation model by correcting it using a linear interpolation, as the current variation is small (current error between the projected current and the verified current range between 1 and 5 %).

The advantage of this approach is that simulations run fast. In an hour, current candidates for every switching frequency and load profile scenario can be found, and with them, the interesting cases can then be validated through the fully modulated simulation. Additionally, once the first simulation is done, its results can be used to test as many scenarios as necessary, and new scenarios can be tested without having to run the first stage, unless the temperature requirements change, or a change to an important device loss parameter is performed (gate resistances, forward characteristics).

On the other hand, the main drawback of this approach is that small prediction errors are unavoidable due to the fact that the prediction model is only good at $T_J \approx 125°C$ and assumes perfect decoupling and steady state after every load change, reason for which the verification runs are a must. An additional consideration is that module models and heatsink models can be decoupled as long as their time constants are far away from each other. Otherwise they can influence the variations of each other and the models cannot be decoupled. However, this is mostly the case between heatsinks and modules, hence problems with this methodology should be very uncommon.

4.2.4 Simulation Results

The presented simulation results were used both for design and final implementation of the converter. There is a difference between the two, as the design and its corresponding implementation were performed with different gate resistances and data. This was a natural result of the nature of the work schedule: at the moment that it was necessary to define the design and start designing mechanical characteristics and ordering parts, no measurements over parallel connected modules had been performed yet, and hence gate resistances from the single module characterization were used to perform the design.

The simulations were subjected to the following conditions:

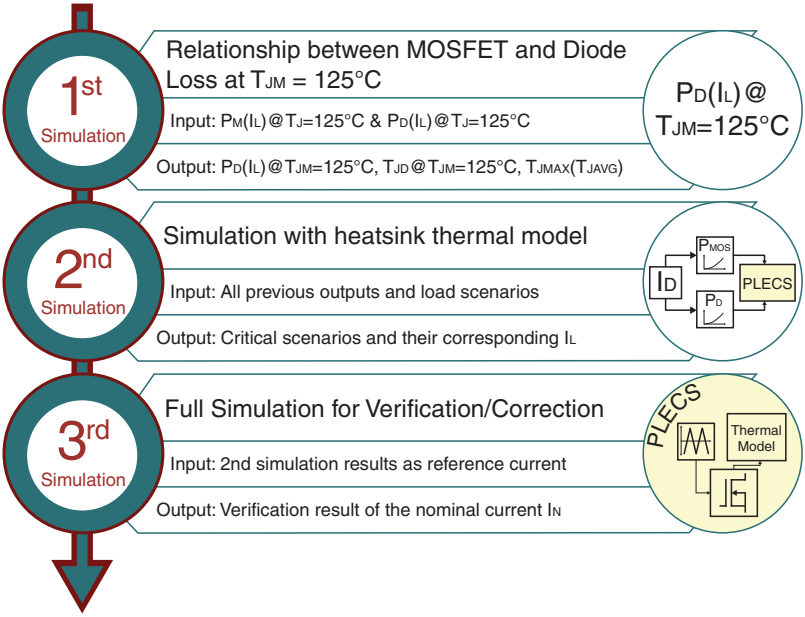


Figure 4.10: Simulation scheme for nominal current calculation based on load profiles.

- Critical modulation index tested for all cases: M = $\frac{2}{\sqrt{3}}$.
- Cos(φ) = [–1 1]. Note that the current is referenced in direction of the grid. Therefore Cos(φ) = 1 is regeneration mode, power from converter to grid, and Cos(φ) = –1 is rectification mode, or power from grid to converter.
- Forward characteristics of the devices were extracted from datasheet available data.
- Switching characteristics were based on experimental data from the characterization experiments.
- The ambient temperature T_{amb} = 45 °C
- The tested gate resistances that were used to design the converter were $R_{G(on)}$ = 0.8 Ω and $R_{G(off)}$ = 0.6 Ω. This resistance pair was used because at the time of design only single device characterization results have been performed. However, after the results of the parallel characterization were obtained, the obtained data was used to performed additional simulations to observe the differences. In this second case, the presented results were obtained using $R_{G(on)}$ = 1Ω and $R_{G(off)}$ = 0.2Ω, which were the characterized resistances from the parallel connection experiments using the gate unit version 3 (GUV3).
- Max. average junction temperature of all devices (MOSFETs/diodes) must

Table 4.6: Converter nominal current used for design purposes for parallel-connected modules using $R_{G(on)} = 0.8\,\Omega$ and $R_{G(off)} = 0.6\,\Omega$, with SPWM modulation with third harmonic injection (equivalent to SVM). Current values in A_{RMS}.

Current	I_T@20kHz
I_N (S2)	197 A
I_{LO}	183 A
I_H	163 A
I_{S6}	137 A
I_{MAX}	275 A
Power	235.4 kVA

not surpass 125°C.

During design, frequencies from 5 to 25 kHz were tested, however it was opted to design the converter with a switching frequency of 20 kHz as this allows the usage of standard core materials for inductors while featuring a switching frequency over hearing range, which is desired from an operation's perspective. In this case, the critical scenario was scenario 2: Strong overload with $\cos(\varphi) = 1$. Under this scenario the nominal current has been determined, and afterwards the other currents were defined in function of it.

The corresponding nominal current result is presented in Table 4.6, and the corresponding junction temperatures for both the MOSFET and the diode are presented in Fig. 4.11.

A closeup of the full modulated simulation results for the MOSFET device is presented in Fig. 4.11. As it can be observed, the average junction temperature almost reaches $T_J = 125°C$, while the $\Delta T_J \approx 22°C$ at the critical point. This peak-to-peak oscillation magnitude reduces drastically when the load current reduces, which is attributed to a small chip total area. This thermal oscillation was discussed with the industry partner, as it is higher that what is typically observed for silicon devices in nominal operation, but it was deemed to be within safe margins. Further research in this topic is nonetheless recommended, as these temperature stresses could have an impact in device lifetime of the device, however its study falls out of the scope of this work.

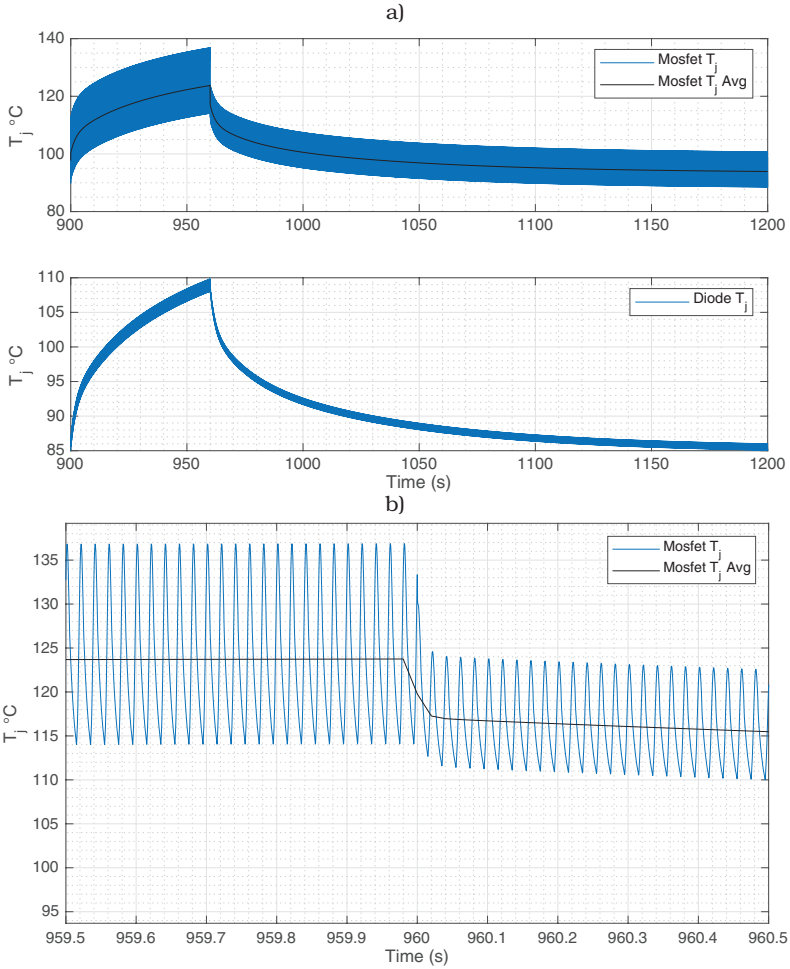


Figure 4.11: Junction temperature of MOSFET and diode while using parallel operated modules in scenario 2, Cos(φ) = 1, M = $2/\sqrt{3}$ while driving 139 A peak per device. a) Junction temperature evolution and its average value during a load cycle in steady state. b) Zoom to the critical junction temperature point at the end of the overload pulse. $R_{G(on)}$ = 0.8 Ω, $R_{G(off)}$ = 0.6 Ω.

Table 4.7: Converter nominal current for parallel-connected modules using the results of parallel-connected characterization experiments. $R_{G(on)}$ = 1Ω and $R_{G(off)}$ = 0.2Ω, with SPWM modulation with third harmonic injection (equivalent to SVM). Current values in A_{RMS}.

Current	I_T@20kHz
I_N (S2)	204 A
I_{LO}	189 A
I_H	169 A
I_{S6}	143 A
I_{MAX}	285 A
Power	243 kVA

Hence, since the determined nominal current of 197 A was verified by the full modulated simulation to comply with the junction temperature requirements, it was defined as the nominal current of the system. However, for design purposes, components were designed for 200 A_{RMS} nominal current (rounded up).

4.2.5 Simulation Results with Parallel Characterized Module Data

After the characterization of parallel-connected modules was performed, further simulations based in its experimental data showed that the differences between the design model and the implemented parallel model configuration, instead of reducing current, could allow to drive slightly higher amounts of current (5 A per device), as it can be observed in Table 4.7 and Fig. 4.12.

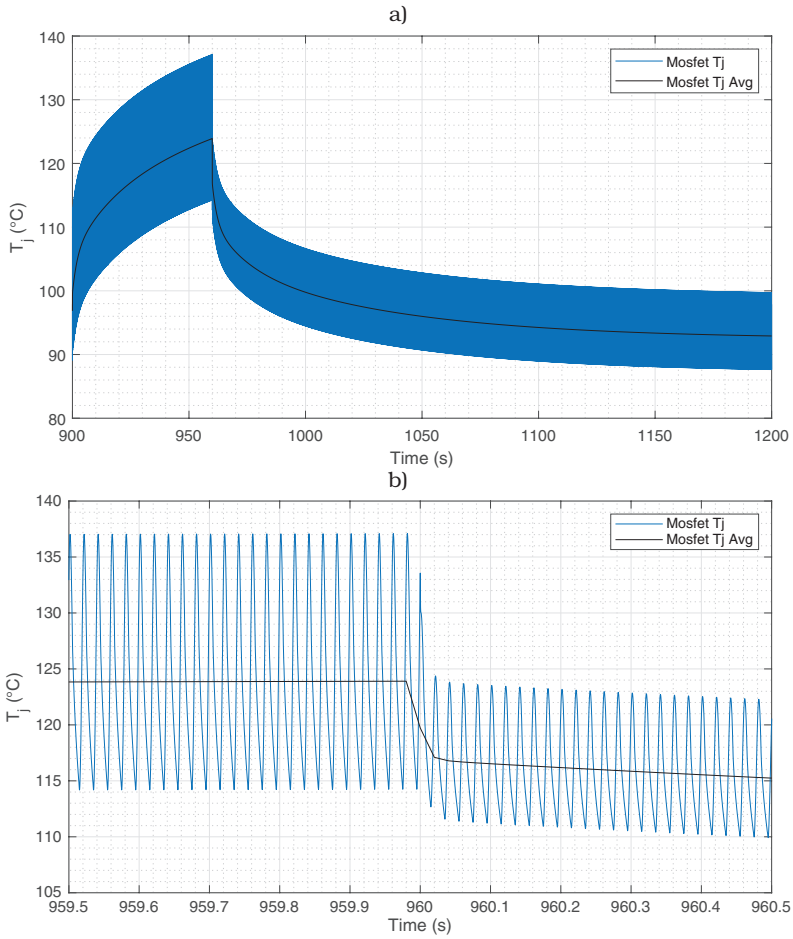


Figure 4.12: Junction temperature of the critical device (MOSFET) under scenario 2, $\cos(\varphi) = 1$, $M = 2/\sqrt{3}$ while driving 144 A peak per device. a) Junction temperature evolution and its average value during a load cycle in steady state. b) Zoom to the critical Junction temperature point at the end of the overload pulse.

Table 4.8: Important converter parameters for the DC-Link design.

Parameter	Value
V_{DC}	1080 V
f_{sw}	20 kHz
Rated power	240 kVA
Grid voltage	690V
Rated current	200A
Modulation	SVM

Therefore, as other parts of the converter were under construction or already designed for 200 A_{RMS}, in light of these new results the nominal current was raised to 200 A_{RMS}, hence being the nominal power of the converter 240 kVA.

4.3 DC-Link Design

The DC-Link has the task of acting as energy buffer and providing a stable voltage for modulation purposes. Additionally, its components can be designed considering several requirements such as voltage ripple, ride-through capability, lifetime, RMS current requirements, reliability considerations, among others. In this section, an overview of the main criteria for capacitance calculations, capacitor selection and bus bar design considerations for the present SiC converter design is presented. Afterwards, the resulting design is summarized and its main characteristics are discussed.

The considered design constraints for the DC-Link of the SiC converter prototype considers the following:

Capacitance wise:

- Allowed DC-Link voltage ripple
- Operation with short grid absence
- Energy to power ratio

Current wise:

- Capacitor RMS current

Voltage wise:

- Rated voltage

Additionally, the capacitors are constrained to fit in the provided rack, add as little stray inductance to the loop as possible (low ESL and good layout design) and operate under the converter design requirements that were previously presented. The relevant design constraints that were considered to have an influence in the DC-Link design are presented in Table 4.8.

Considering the capacitor technology, a short summary of the differences of main capacitor technologies can be observed in Fig. 4.13, where Al-Caps are Aluminum based electrolytic capacitors, MPPF-Caps are Metalized PolyPropylene Film Capacitors (film) and MLC-Caps are Multilayer ceramic capacitors.

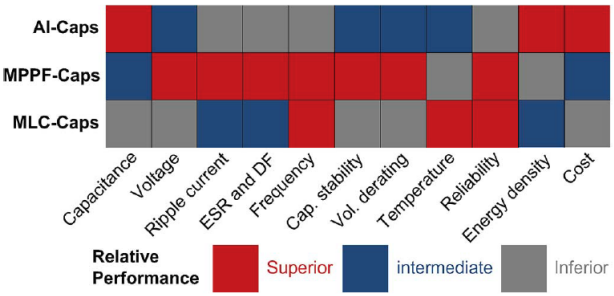


Figure 4.13: Summary of advantages and disadvantages of capacitor technologies for DC-Link purposes. ©2014 IEEE. Source: [19].

Due to their reliability advantages, reduced ESR, high rating voltages and superior stray inductance performance, film capacitors were more suitable than the alternatives for the present converter design, which although not standard for this application, they are not uncommon according to the industry partner.

4.3.1 DC-Link Requirement Criteria

Capacitance Requirements

- Minimum DC-Link Capacitance value for defined Voltage ripple in a 3Ph-2L inverter

  To calculate the minimum capacitance required to have a defined amount of ripple, the analysis of the current ripple in one switching cycle for the worst case scenario of converter operating conditions must be performed in order to determine the smallest capacitance that complies with this Voltage ripple. A thorough analysis for the 3Ph-2L inverter is presented in [87], and starts with defining the capacitor for a determined voltage ripple as:

$$C_{DC} = \frac{i_{cap}dt}{\varepsilon V_{DC}} \tag{4.9}$$

  in which ε is the voltage ripple in percentage. The objective is to determine $i_{cap}dt$ max (which in [87] is defined as $Asec_{max}$) in one switching period for the worst case scenarios of power factor and modulation index. After normalizing, $Asec_{p.u.} = \frac{Asec}{\sqrt{2}I_N T_{sw}}$, [1] and analyzing this expression under all possible power factors and modulation indexes, the maximum possible $Asec_{max_{p.u.}} = 0.25$. Therefore:

$$C_{DC} = \frac{0.25\sqrt{2}I_N T_{sw}}{\varepsilon V_{DC}} \tag{4.10}$$

[1] I_N is nominal current, T_{sw} is switching period

which is also derived in [88].

Hence, regarding the test setup main parameters, the absolute minimum DC-Link capacitance value to accomplish a determined amount of ripple such as, for example, 5% ripple on the DC-Link voltage without perturbations and normal grid conditions would be C = 62 μF.

- Operation with short grid absence (ride through)

  In this case, the DC-Link capacitance requirement is that the capacitor does not drop below a certain voltage for a defined time without grid. It was agreed with the industry partner, that the DC-Link voltage should not drop below 650 V after 3 ms in this scenario, as a lower voltage in this conditions would force shutdown by the control platform.

  To determine the required capacitance, the converter can be modeled as a capacitor with a constant power consuming load $i_L(t) \cdot V_L(t) = K$ where K is the constant power consumption value. Therefore, by using current and voltage Kirchoff equations:

$$K = C\frac{dV_c(t)}{dt} \cdot V_c(t) \tag{4.11}$$

$$K = \frac{C}{2}\frac{dV_c^2(t)}{dt} \tag{4.12}$$

Replacing $V_c^2(t)$ for X(t), it yields:

$$K = \frac{C}{2}\frac{dX(t)}{dt} \quad /\mathcal{L} \tag{4.13}$$

$$\frac{2K}{sC} = (sX(s) - X(0_-)) \quad /\mathcal{L}^{-1} \tag{4.14}$$

$$X(t) = \left(\frac{2Kt}{C} + X(0_-)\right)\mu(t) \tag{4.15}$$

So, for any $t > 0$:

$$C = \frac{2Kt}{X(0_-) - X(t)}. \tag{4.16}$$

Therefore, considering that after 3 ms the voltage should drop from 1080 V to a maximum of 650 V the corresponding capacitor is calculated as in expression 4.17.

$$C_{DC} = \frac{2 \cdot 240000 \cdot 0.003}{1080^2 - 650^2} = 1.94\,\text{mF} \tag{4.17}$$

- Energy to power ratio

  Based on a revision of several commercial power converters, a standard ratio of energy stored in the DC-Link and nominal power in the converter has been observed. The ratio for medium voltage drives with film DC-Link capacitors

is about $\tau_{E/P}$ = 8 ms = 8 J/kVA = 8 Ws/kVA, and although conservative, leads to a DC-Link capacitance that complies with standard design practices for silicon-based power converters. Therefore, for this particular converter characteristics:

$$C = \frac{2S \cdot 8 \cdot \tau_{E/P}}{V_{DC}^2} \tag{4.18}$$

Where S is the nominal rated power of the converter in VA.

Using (4.18) and the converter parameters of Table 4.8, the nominal power of the converter and the nominal DC-Link voltage, the DC-Link capacitance according to this criteria is: C_{DC} = 3.29 mF.

RMS Current Requirements

- Analytical calculation of the Capacitor RMS current

  As it can be found in [89], a thorough analytic deduction of the DC-Link RMS current of a 3Ph-2L converter has been made. From it, the main conclusions of the work are that a good first order approximation for a 3Ph-2L inverter with PWM modulation with third harmonic injection (equivalent to SVM) and high modulation indexes (such as induction motor and active rectifier applications) is that:

$$I_{C_{RMS}} = I_{ac_{RMS}} \cdot 0.5 \tag{4.19}$$

  Hence, since typically in industry each converter features their own DC-Link (for example, a back-to-back converter is built by connecting two converter modules through their DC-Links), it would be enough for this design to consider (4.19), hence yielding I_{DC} = 100 A RMS.

  This approximation was deemed acceptable, as film capacitors can withstand high RMS currents, hence it is expected that RMS current was not going to be a design constrain.

Rated Voltage Requirements

Regarding rated voltage it should be enough in low ripple applications (such as a DC-Link) that the rated voltage is superior than the DC-Link voltage. However this is not a hard requirement, as in film capacitors operation over the rated voltage will only impact capacitor lifetime along with temperature, and can be used if the capacitor temperature is considered accordingly. On the other hand, overshoots can be withstood with ease, as film capacitors are typically capable of withstanding overvoltages of up to twice the rated voltage [90].

Summary of Calculations According to the Defined Criteria

The calculated values applied to the particular task at hand are summarized in Table 4.9.

Table 4.9: Summary of design criteria results for the DC-Link capacitor bank.

Calculation	Parameters	Result
Ripple	5%	C = 62 µF
Ride through	t_p = 3 ms	C = 1.94 mF
$\frac{kWs}{kVA}$ ratio	$\tau_{E/P} \approx 8$ ms	C = 3.29 mF
I_{cap} RMS	none	I_{cap} = 100 A

Therefore, the minimum requirements for the capacitor bank were the following:

- C_{min} = 1.94 mF
- Min. I_{cap} = 100 A
- $V_{rated_{min}}$ = 1080 V

These results have been discussed with the industry partner, and from the obtained conclusions it was determined that although the minimum capacitance according to the corresponding requirements is 1.94 mF, over 2.2 mF would be desired from their point of view, while 3.3 mF would result in a good practice conservative design.

4.3.2 DC-Link Implementation

DC-Link Capacitor Selection

To choose a complying capacitor bank, the capacitors had to be chosen considering also space constraints in the rack. The available space for the DC-Link capacitor bank is, in length x width x depth terms: 15.6 x 74.7 x 14.4 cm^3. See Fig 4.14.

In order to put several capacitors in parallel, and considering available radial options of film capacitors in the market, the options were to use capacitors of diameter [6, 7.5, 10] cm (8.5 cm was discarded because it led to excess wasted space). From a parasitic elements perspective (ESR, ESL) it is best to have several in parallel and therefore 7.5 cm capacitor solutions were chosen.

Constrained to these limits, several capacitors from AVX, ICAR and Elecronicon have been considered as candidates. From them, the AVX FFLI6U0157K [91] has been selected, its corresponding data can be found in Table. 4.10.

DC-Link Bus Bar Design

For the construction of the DC bus bars, the connection points to the output DC bars, and to the modules were constrained by the rack, as well the capacitor position due to the available space. An alternating pattern for the capacitors has been selected, as it can be seen in Fig. 4.15 because it has been observed in simulations that it presents stray inductance advantages. Additionally, it has been decided to fill the DC-bank with capacitors, as this provides a better layout from a symmetrical perspective to obtain low stray inductance values when observed from the module connection terminals. The copper bars were made

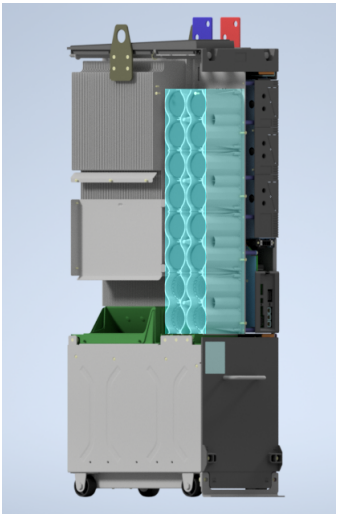


Figure 4.14: Volumetric space of available room for the DC-Link capacitor bank in the rack. Dimensions: 15.6 x 74.7 x 14.4 cm^3

1.5 mm thick, and were separated through a 0.25 mm Hostaphan RN foil, capable of isolating 19 kV at this thickness. This design was then analyzed through INCA 3D (nowadays called Altair Flux), which is a software that uses partial element equivalent circuit methods (PEEC) to analyze the 3D model considering the capacitor ESL to calculate the stray inductances observed from the different terminals. This software was used to determine the observed stray inductance of the DC-Link from the terminals of the modules, resulting for each module terminal from 1 to 6: [12.8 12.3 12.1 12.2 12.3 12.8] nH respectively. This results in an average approximated stray inductance of $\approx$ 12.4 nH.

Table 4.10: AVX FFLI6U0157K capacitor characteristics.

Parameter	Value
Manufacturer	AVX corporation
Model	FFLI6U0157K
Nominal Voltage	1150 V
Capacitance	150 µF
Max RMS current	46 A
Dimensions	d = 75 mm, h = 105 mm
ESL	35 nH
ESR	4.2 mΩ
R_{th}	4.5 K/W

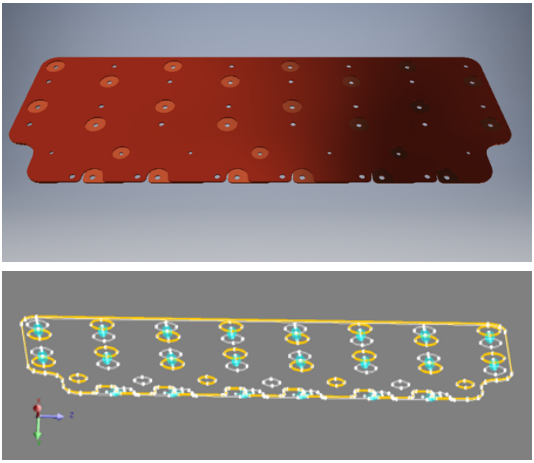


Figure 4.15: Up: 3D model of the 16 capacitor DC-Link bus bars. Down: INCA 3D stray inductance analysis.

Table 4.11: DC-Link design summary.

Parameter	Value
C_{eq}	2.4 mF
Capacitors	16, all parallel connected
Estimated stray inductance	12.8 nH
Max RMS current per cap.	6.25 A
Max DC-Link RMS current	100 A
$\frac{kWs}{kVA}$ ratio	5.832 ms

4.3.3 DC-Link Design Summary

Finally, and considering the characteristics of the 16 capacitor bank under this physical construction design, a table summary of its main attributes is presented in Table 4.11.

4.4 LCL-Filter

The LCL-Filter has the main task of keeping harmonic emissions in compliance with grid-codes and standards. For this converter, an LCL-Filter with active damping has been implemented. This filter is part of the dissertation of Marcus Mueller, and therefore will not be tackled here in detail. However, the main considerations, constraints and resulting components are summarized here.

4.4.1 Requirements and Constraints

The LCL-Filter has the following requirements and conditions:

- The LCL-Filter has to be designed for a switching frequency f_{sw} = 20 kHz and a nominal current of 200 A_{RMS}.
- The LCL-Filter has to be designed considering active damping control algorithms.
- The LCL-Filter has to be designed with a high resonance frequency in the 6 kHz range, to not be affected by other converters in the network if the LCL-filter is left connected to the grid without powering the converter.
- The LCL-Filter has to comply with the IEC/TS 62578 grid-code harmonic standard. Important remark is that both this harmonic standard and the EN61000-2-2 contain mostly recommendations for harmonic emissions in the line-line voltage at the point of common coupling. Thus, the observed harmonics in the line-line voltage at the point of common coupling were the main concern and design constrain for harmonic emissions.

Additionally, the filter considered the following:

- Limit the current to not surpass the i^2t capability of the Diodes under low voltage ride through (LVRT). This constrain limits the lowest limit of inductance values for filter design.
- Grid model over 2 kHz does not behave like an inductor, and considering that it does so would increase the size of the inductors. Hence a more accurate model for the grid impedance based on the CISPR11 EMC standard [92] and the IEC/TS 62578 has been used, which is based on measured grid data.

Under these considerations, the approach to design the filter was performed in the following steps:

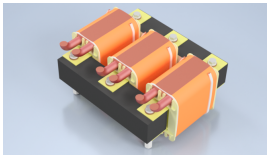
1. Use the grid impedance model with the filter model to determine the impedance observed at the point of common coupling as a function of frequency.
2. Several simulations are performed using different power factors, modulation indexes and grid voltage variations to determine a theoretical worst case spectrum. This spectrum does not represent any operation point, but it summarizes the highest emissions among all cases.
3. A parametric search within reasonable L and C values is performed (leaving aside LC combinations that do not comply with resonant frequency), and the grid-codes are used to determine possible filter results.
4. Possible results are then filtered by what manufacturers are capable to achieve, while considering minimizing filter stored energy and considering i^2t diode limitations.

Following this design methodology a filter was designed to comply with the converter requirements, resulting in the information presented in Table 4.12.

Table 4.12: Filter parameters of the corresponding filter design.

Parameter		value	p.u.
Grid-side inductance	L_N	75 µH	1,2%
Converter-side inductance	L_{SR}	75 µH	1,2%
Condensator	C_F	20 µF	1,3%
Resonant frequency	f_{res}	5,5 kHz	
Ripple current (RMS)	I_{PWM}	16 A	8%

Table 4.13: Inductor characteristics.

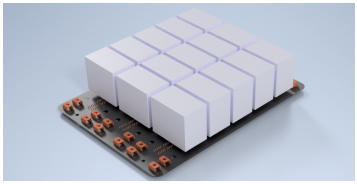
Parameter	Value	3D render of the inductor
Manufacturer	Schmidbauer	
Material	laminated steel, 0.1mm	
I_N	200 A	
Cooling	Forced, 4 m/s	
Weight	22 kg	
Volume	12 dm^3	
Inductor value	75 µH	
Quantity	2 (converter side and grid side)	

4.4.2 Filter Implementation

Regarding the implementation of the filter, several manufacturer options were considered. Filter manufacturers did not have off-the-shelf solutions for the required switching frequency and nominal current, and hence they proposed different designs for the inductors instead, using different core materials as well within the realm of their particular expertise. However, for the required operation point the most attractive offer came from the company Schmidbauer, which presented an inductor realization proposal using an electrical steel laminated core with very thin layers, of 0.1 milimeters thick. A summary of the characteristics of the manufactured inductor and its 3D rendered implementation can be found in Table 4.13.

On the other hand, capacitors from the company TDK were selected to provide the capacitive part to the filter. These capacitors have been selected to be snubber capacitors due to their high ripple current capability while also presenting small capacitance values. This was an important requirement for the LCL-filter in order to present a high resonant frequency, which was a requirement from the industry partner. The capacitor bank was built with 5 parallel-connected capacitors per leg in star configuration. However, in the physical implementation, capacitors could be bypassed to vary the capacitance of the bank for experimental purposes. Information related to the selected capacitor and its corresponding implementation can be found in Table 4.14.

Table 4.14: Filter capacitor characteristics.

Parameter	Value	3D model of the capacitor bank
Cap. Manufacturer	TDK	
Model	C4BSMBX4500Z_N	
Type	Film, Snubber	
Nominal V_{AC}	550 V_{RMS}	
Capacitance	5 µF	
I_{RMS}	42 A	
Capacitors in the Bank	15	
Capacitors per phase	4 (adjustable)	

4.5 The SiC Converter Demonstrator

4.5.1 Summary of Converter Design Parameters

After all parts of the converter were designed, components were ordered and the construction of the converter rack, filter rack and safety cabinets was performed. A summary of the resulting converter parameters can be found in Table 4.15.

As previously mentioned, the converter was built using the racks provided by the industry partner. The first rack containing the converter itself can be found in Fig. 4.16. There, the three pairs of modules with their corresponding gate units can be found in the center of the converter on top of the heatsink, while the AC side connections appear on the right. On the left side, the low inductive 2.4 mF DC-Link capacitor bank has been mounted, and its DC-side connection can be found on top. All communications between the rack and the control platform, including gate signal pulses, were performed through optic fiber. The DC-Link voltage was measured using a voltage divider attached to a $\Delta\Sigma$ converter, in-module temperature was measured through the module's NTC resistor, and it was sent to the control platform along an error signal which is available for a future shortcircuit detection module to communicate if the gate unit detected such an event.

Regarding the LCL-Filter rack, a 3D model of its implementation can be found in Fig. 4.17. The same form factor of the rack has been used to mount the filter, but the heatsink has been removed to mount the inductors, leaving only the fan to provide forced cooling. The filter also considers 6 LEM LF-510-s current sensors to feedback the three converter side currents and the three grid-side currents to the control platform. This is also performed through $\Delta\Sigma$ converters. Additionally, the grid voltages were measured through voltage dividers which communicated their readings through $\Delta\Sigma$ converters to synchronize control signals with the grid voltage through Phase Locked Loops (PLLs). Hence 9 optic fiber cables return to the control platform. Since $\Delta\Sigma$ converters need to be powered as well, a slot for power sources has also been mounted in the rack as it can be observed in the figure.

Finally, regarding mechanical considerations, isolation considerations were taken as presented in [93]. According to it, and to the voltage range that the converter operates, the defined surge voltages and overvoltages for the converter

Table 4.15: Summary of final design parameters of the SiC converter demonstrator.

Main Specs	Grid voltage V_{LL}	690 V
	Phase current I_N	200 A
	Nominal power S	240 kVA
	Switching frequency f_{sw}	20 kHz
DC-Link	DC-Link capacitance C_{DC}	2.4 mF
	Nominal DC-Link voltage V_{DC}	1080 V
	Characteristics	Film based, symmetric, low inductive ($\approx$ 12.4 nH)
LCL-Filter	Converter side inductance L_{SR}	75 µH
	Grid side inductance L_N	75 µH
	Filter capacitance C_F	20 µF
	Characteristics	0.1 mm electrical steel inductors, and 5.5 kHz resonant frequency
Cooling	Type	Forced cooling, fan PWM controlled Heatsink provided by industry partner
Build	Rack	Provided by manufacturer
	Norm	Rack built according to DIN EN 61800-5-1

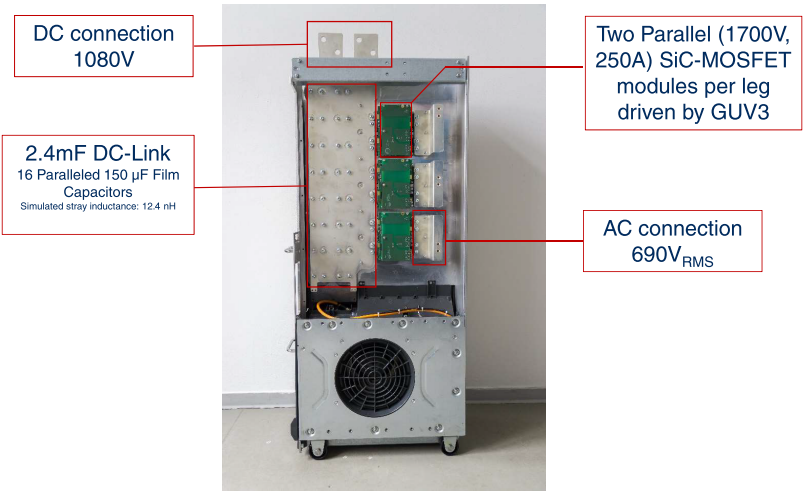


Figure 4.16: Picture of the SiC converter demonstrator right after ending construction.

are 8000 V and 3110 V respectively. With these voltages, clearance and creepages can be obtained by following what is stipulated in the corresponding tables in [93], which were built using basic isolation considerations (surge voltage corresponding values) for all parts of the converter with the sole exception of the DC-Link plates, which only present functional isolation. The corresponding clearance and creepage values according to the basic isolation scheme are 8 mm in both cases, and for the functional isolation 3.4 and 5.5 mm respectively.

Finally, the connection to the grid was achieved by the usage of a transformer which provided 400 V_{ll} from the medium voltage grid. The whole system including the SiC converter rack, LCL-Filter rack, EMC-Filter and grid connection can be found in Fig. 4.18.

Important considerations regarding converter construction are the following:

- The SiC converter demonstrator has been built with a different heatsink that the one the model was to represent, being the heatsink of this rack substantially better than the design model. Thus, the temperatures of the testbench are cooler than the ones predicted by the models. The present heatsink model is confidential, hence is not presented here. However, operation under reactive power and nominal current has shown that the simulation predicts the corresponding temperatures with acceptable accuracy. This can be observed in Table 4.16, where the cooling represents the percentage of the total speed of the fan at which the converter was operated. As it can be observed in the table, the simulation model procedure predicts the steady state temperature of the case very well. However, as it can be observed, the converter runs relatively cold. Hence it is considered overdi-

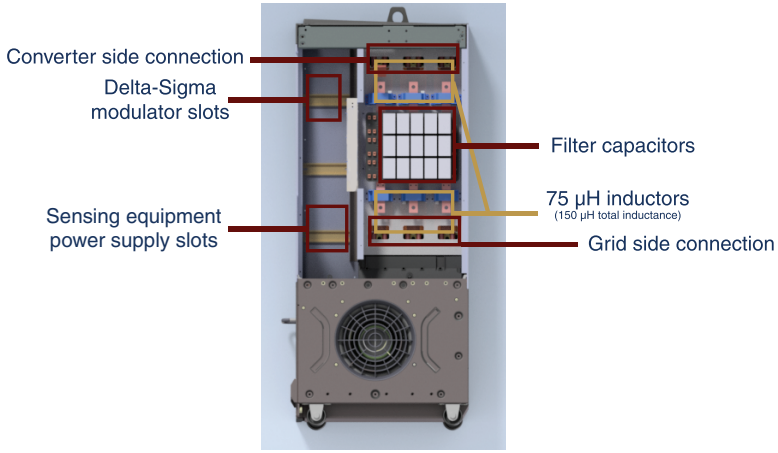


Figure 4.17: 3D model of the LCL-Filter rack containing the grid-side inductor, the converter side inductor, and the capacitor bank for the LCL-Filter implementation.

mensionated in that regard. This implies that the converter is not directly comparable with similarly rated converters on the market.

Table 4.16: Measured and predicted temperatures by the simulation model for $\cos(\varphi) = 0$, $M = 0.6024$ and $I_N = 200\,A_{RMS}$.

Cooling	Measured T_{NTC}	Simulated T_{case}
25%	55°C	56.3°C
75%	45°C	47.2°C

- When putted into operation, the converter presented common mode issues (differential current breaker kept opening the circuit), and hence an EMC-Filter was necessary to be added to the setup. This was a functional solution and the study and considerations of an EMC-Filter were not in the frame of this work, hence it has been marked as an unsolved issue, worth investigating as future work.

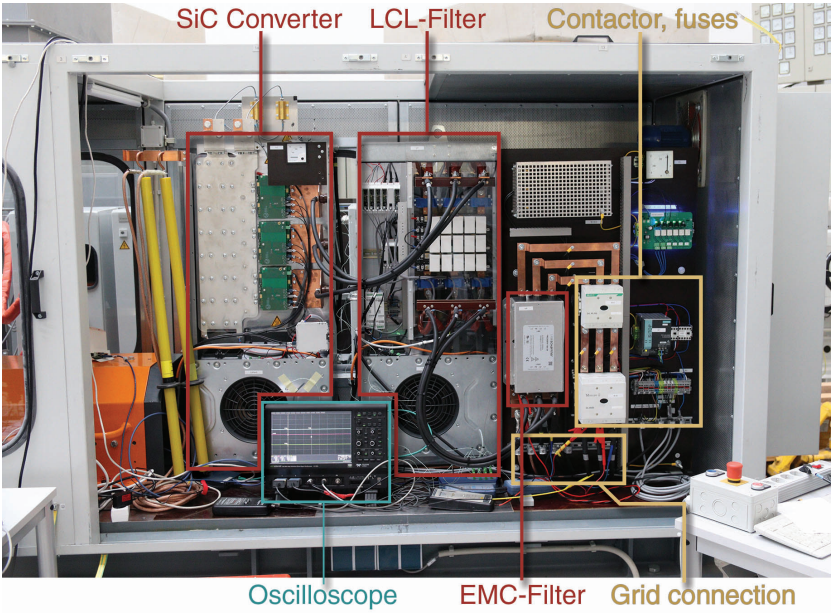


Figure 4.18: SiC converter demonstrator testbench. From left to right: SiC Converter, LCL-Filter, EMC-Filter, safety equipment and grid connection.

4.5.2 Control and Measurements

The converter was then controlled by using the control platform of the TU-Dresden's chair of power electronics, which is based in the Xilinx Zynq family, particularly the 7010 SoC, running the control algorithm at 40 kHz. All signals between the control platform and the demonstrator were sent and received through optic fiber, while the connection between the control platform and the computer running the HMI was performed through ethernet. The oscilloscope was controlled remotely using the same protocol. A picture of the control platform can be found in Fig. 4.19, where the expansion cards for optic fiber emitters can be found on the left side, while the right side was in charge of data acquisition.

Meanwhile, the implemented control algorithm to control the setup is Voltage Oriented Control (VOC) with Sinusoidal Pulse Width Modulation (SPWM) and active damping. Voltage oriented control consists in synchronizing the control scheme with the grid voltage by measuring its phase, in this case through phase locked loops (PLL), to then use the synchronized angle to rotate the $\alpha\beta$ vectors (current and voltage vectors) to a rotating dq frame. Here the grid frequency is observed as a constant value and therefore classic PI controllers can be used to control the voltage magnitudes without steady state errors. Additionally, the

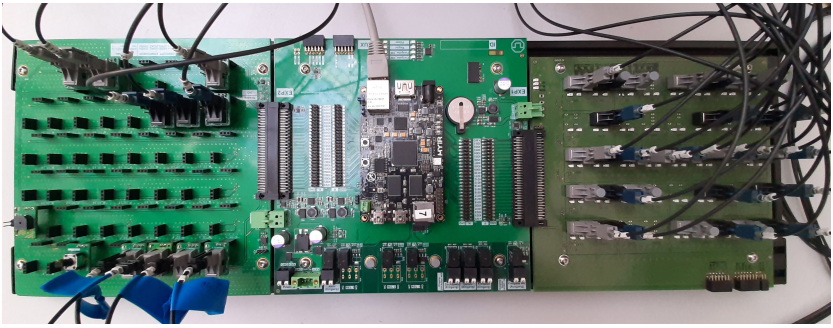


Figure 4.19: TU-Dresden's chair of power electronics control platform, based on the Xilinx Zynq 7010 SoC (FPGA + 2CPU cores).

control scheme included an active damping control algorithm to damp the resonant frequency of the LCL-Filter. To achieve this, a virtual resistor is supposed, and the control algorithm is operated through the current of the filter capacitor ($I_{SR} - I_N$) to simulate this resistance through converter voltage actuation, hence damping the resonant frequency [94]. The control scheme can be found in Fig. 4.20. Please note that the referred current i_s is the grid current vector, in other words, i_N after Clark $\alpha\beta$ transformation.

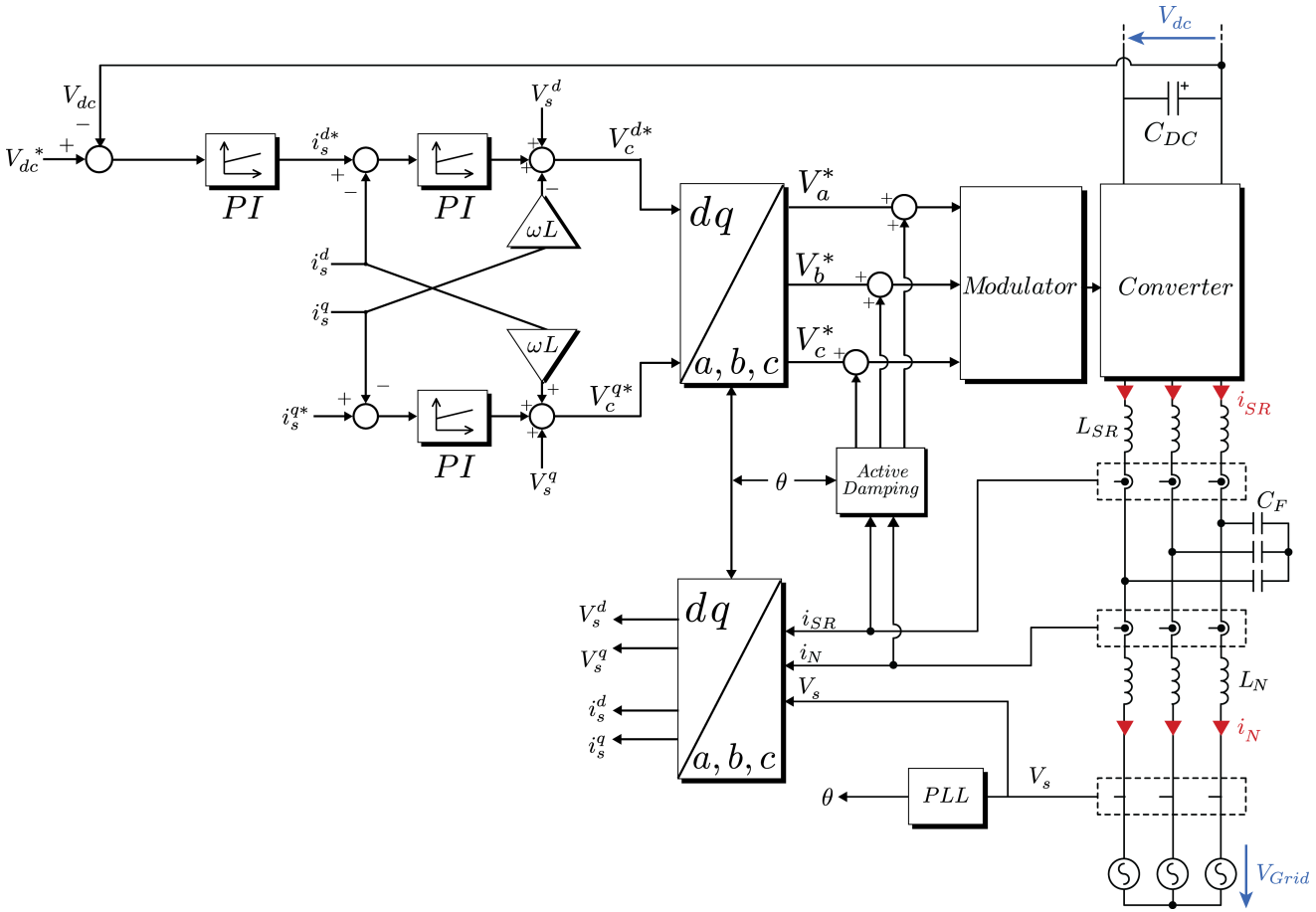


Figure 4.20: Control Scheme for the SiC converter demonstrator while connected to the grid.

4.5.3 Experimental Results

In the present section, results validating the correct operation of the converter are presented. The converter has been put into operation in several steps, which were:

- Modulation test: The converter has been operated without load to verify the correct operation of the legs and the capability of switching the output voltage correctly. Schematic described in Fig. 4.21.a.
- Fence test: An inductor has been used in every leg to load current in it and then freewheel it through the diode. This can be interpreted as a several pulse test analog to a double pulse test, to drive currents close to the nominal current through every leg to verify their current driving capability. Schematic described in Fig. 4.21.b.
- RL-load: A resistive load and the filter inductors have been used to test the converter current loop. The test was however limited as the resistive bank consumes active power and hence, due to the power limit the DC-source could provide to the DC-Link this test was limited to very low currents. Schematic described in Fig. 4.21.c.
- Grid connected converter with reactive power: The final test consists in operating the converter with grid connection to verify the capability of the converter of controlling current and voltage while also complying with the corresponding standards. However, due to the fact that it was not possible to go to the test facilities of the industry partner to test the converter with active power, it was agreed for the converter to be tested in the University while driving nominal current with reactive power as a compromise. Schematic described in 4.20.

To validate the operation of the converter, only the most relevant waveforms are shown. The measurement probes are presented along their relevant measured variable in Table 4.17, and were measured by using a 12bit Lecroy HDO6054-MS 500 MHz oscilloscope.

Table 4.17: Testbench measurement instruments.

Variable		Probe	Bw
Line-Line grid voltage at the PCC	V_{ll}	Testec TT-SI 9110	100 MHz
Upper MOSFET voltage measurement	V_{DS}	PMK Bumblebee	300 MHz
Current before the EMC-Filter	I_N	PEM CWT 15B	16 MHz
Converter current	I_{SR}	PEM CWT 15B	16 MHz

Converter With Nominal Current Operation and Reactive Power

To test the converter functionality, the converter was connected to the grid and operated with nominal current and reactive power for over 45 minutes at a time. First, the corresponding signals captured by the control platform at 40 kHz while being received at that frequency from the $\Delta\Sigma$ converters are presented (currents were measured at 200 kHz to reduce delay and make a more robust active damping algorithm at the cost of lower signal resolution). As it can be seen in Fig. 4.22,

the V_{DC} voltage is controlled accurately by the control platform, presenting less than 0.4% voltage ripple and remaining otherwise constant. On the other hand, the three phase currents measured by the controller present nominal amplitudes, and the the typical current shape and phase distribution of a three phase system, while showcasing the harmonic reduction of the grid side current I_N performed by the LCL-Filter. Finally, it can be observed when comparing the PCC phase voltages (against ground) and the current, that the phase shift between both signals is correctly adjusted to $\frac{\pi}{2}$, aligned with the desired operation point.

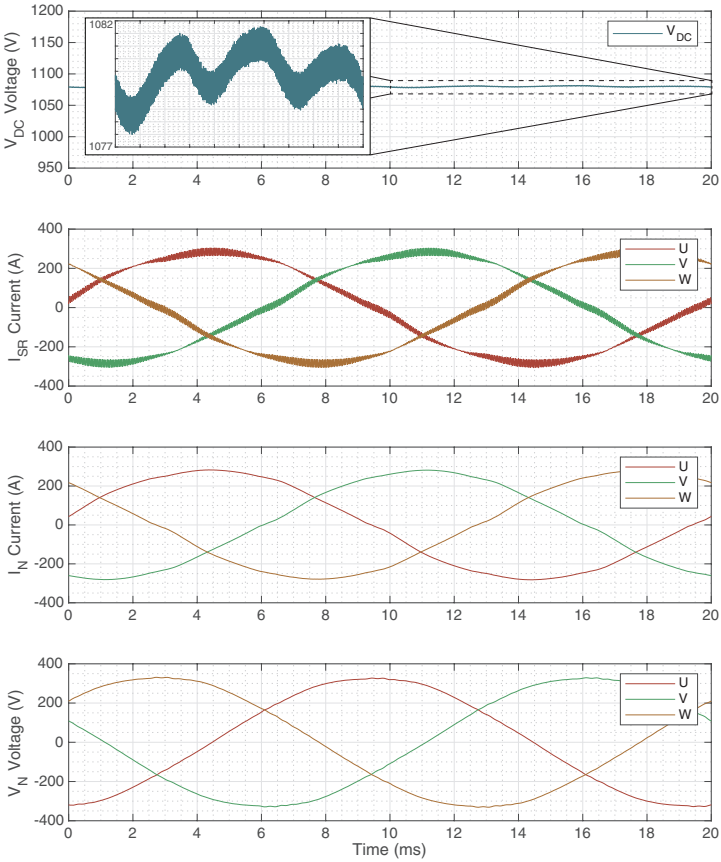


Figure 4.22: Converter DC-Link voltage, grid voltages (U, V, W) and grid currents (U, V, W) as measured by the control platform at 40 kHz (shown converter currents is oversampled at 200 kHz). From top to bottom, the presented signals are: 1st) DC-Link voltage, with zoom in the [0.01 0.02] s timespan. 2nd) Converter current I_{SR} before entering the LCL-filter. 3rd) Grid side current I_N after coming out of the filter. 4th) Grid phase-neutral voltages (at the PCC.)

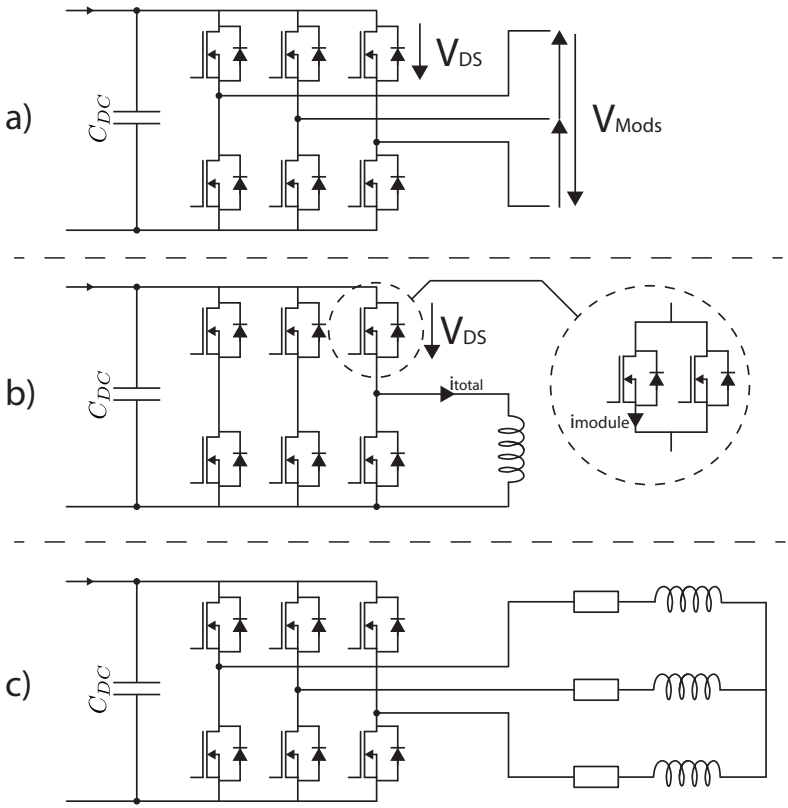


Figure 4.21: Description of the experimental steps that were taken to verify correct operation of the converter before performing grid-connection. a) Modulation test, b) Fence test, c) RL load test.

To observe the currents with more resolution and adequate bandwidth, Rogowski coils have been used and with them the corresponding current spectrum has been calculated by using five signal periods, as it can be seen in Fig.4.23, which also present the corresponding signals in time. In there, it can be observed that both current signals (before and after the LCL-Filter) present significant high frequency noise, which is far beyond the considered frequencies by the norms for harmonic emission, being instead part of the EMI spectrum and hence requiring an EMC-Filter. However, for the purposes of this work, as this filter was not part of the study, the signals have been filtered by software with a low-pass filter with a cut-off frequency of 150 kHz to show the effectiveness of the LCL-Filter and corresponding design. The LCL-Filter is able to achieve significant reduction in current harmonics up to 25 times in the first carrier frequency bands as it can be observed in the corresponding FFT.

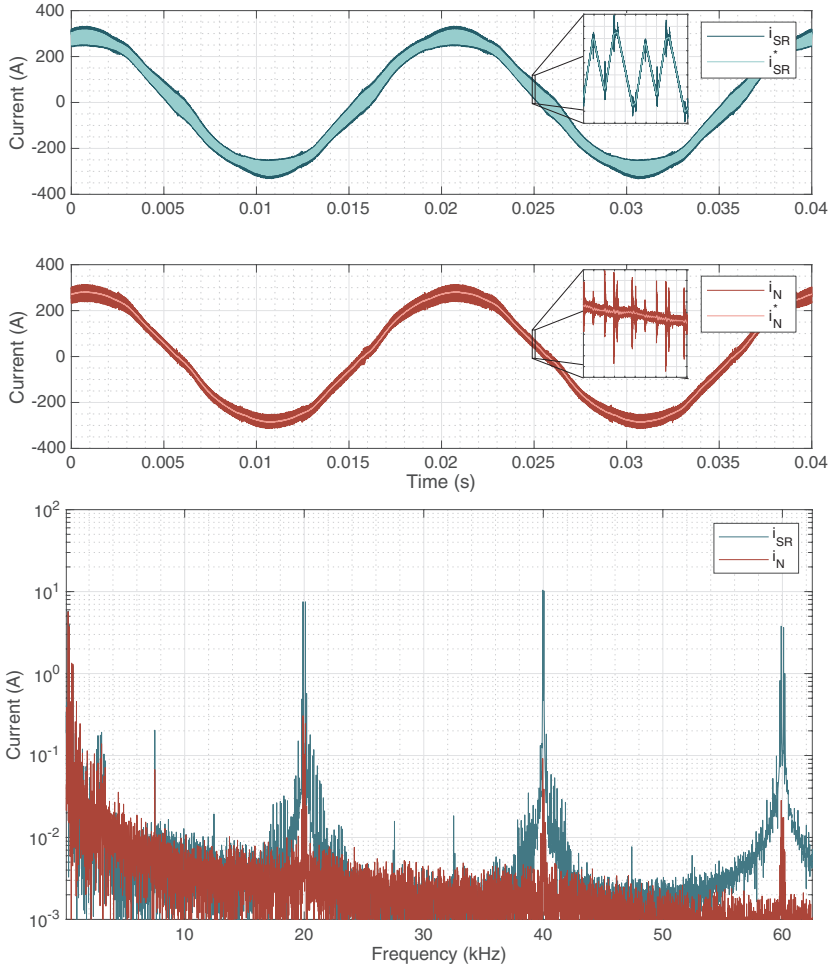


Figure 4.23: Output current harmonic emissions before and after the LCL-Filter. Up: Signals vs time, asterisk signals are filtered with a low-pass filter with a cut-off frequency of 150 kHz. Down: FFT of the corresponding unfiltered current signals.

However, as mentioned in the filter design section, the compliance with grid-codes is in this case defined by the line-line voltage at the point of common coupling. Hence, the line-line voltage spectrum at the point of common coupling has been compared with the corresponding limits of the different standards, as it can be observed in Fig.4.24. There, it can be appreciated that the converter complies with both proposed grid-codes successfully for this operation point. Note that the compliance with the EN61000-2-2 norm in this case was influ-

enced by the actual grid impedance of the experimental setup, as the filter has not been designed to comply with this norm at all times.

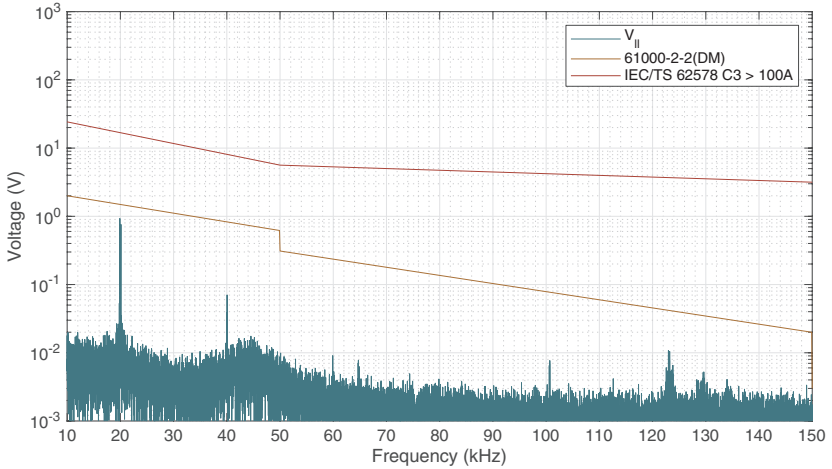


Figure 4.24: Output voltage harmonic emissions (differential mode) of the line-line voltage at the point of common coupling and the corresponding relevant harmonic standards.

Finally, the voltage across the upper MOSFET of one leg has been measured to ensure that the overvoltages are within safe margins. The corresponding results can be found in Fig. 4.25, where it is observed that even in the worst case scenario, the maximum observed overvoltage in the MOSFET reaches 1265 V, hence deemed safe for continuous operation.

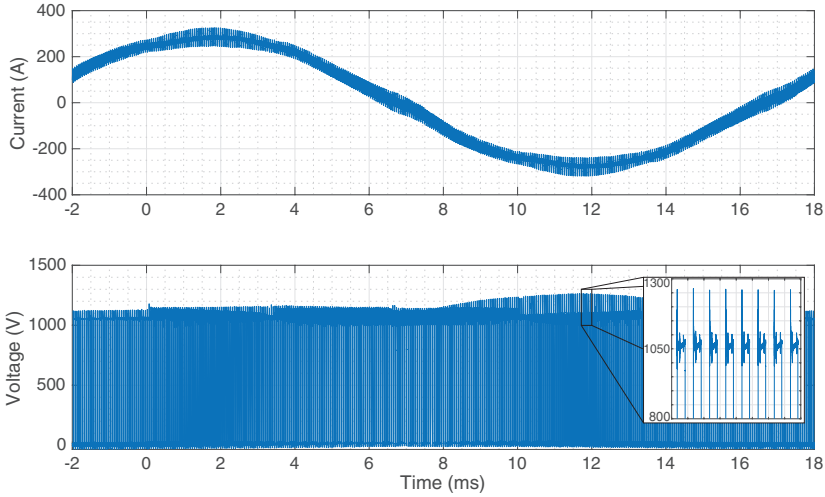


Figure 4.25: MOSFET V_{DS} voltage and leg driven current for a single period.

Module Current Sharing

Additionally, an important fact to verify during converter operation was the capability of module parallel operation. In other words, to verify that the modules in a leg were sharing the current properly. By characterization experiments it was already determined that differences should be small, but it remained to be tested how good they could behave in converter operation. After 45 minutes of operation, measurements were performed and its results are shown in Fig. 4.26. In the figure, the converter current and the current through the upper module are shown, presenting almost exactly half the current of the parallel connection. This means that only a small to close to almost no de-rating may be possible with these SiC modules in this parallel-connected configuration, hence validating that SiC module parallel connection is feasible with close to zero de-rating requirements.

DC-Link stray inductance approximation

Finally, it was important to verify that the overvoltage observed by the devices is within safe margins for all possible conditions (in other words, that the added stray inductance is within acceptable range). To that end, results from the fence tests are presented in Fig. 4.27. In this test, a single inductor was connected as load to a single leg of the converter (two modules in parallel), and this leg was pulsed as in a double pulse test, but with several pulses until the desired current was reached. Currents up to 400 A peak per leg were tested on the three legs, and the voltage over the upper switch device was measured. Since the module connection terminals of the converter were designed to minimize stray induc-

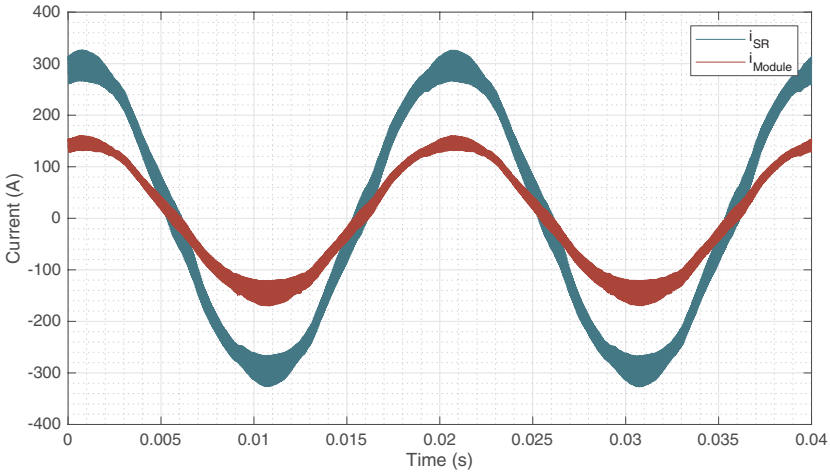


Figure 4.26: Module current sharing behavior measured in a single leg. Signals were filtered at 150 kHz.

tance and therefore did not consider space or terminals for a shunt resistor, only Rogowski coils were an option to measure the current through the modules. The used Rogowski coils are the CWT 15B, and have a bandwidth (16 MHz), which is not large enough to observe all signal characteristics, but had been tested in the DPT testbench to be enough to capture the increase and decrease of the current during transients. Using them, an estimation of the maximum observed voltage and the worst case scenarios for di/dt measured for this module can be used to obtain an estimation. The signals corresponding to the experiment can be found in Fig.4.27. Here, as it can be observed, only an overvoltage of 260 V is observed by switching 400 A through the leg (hence 200 A per module). This voltage is generated by half of the current through the module impedance (approx.), plus total of the current through the DC-Link stray inductance. Using this result, the stray inductance of the DC-Link can be estimated as the measured overvoltage minus the stray inductance related overvoltage of a single module as a result of its (7 A/ns at ambient temperature and 200 A) and then divide the total through the added di/dt of both (which is the DC-Link di/dt current variation):

$$L_{DC} = \frac{260\,V - 7\,A/ns \cdot 13.3\,nH}{14\,A/ns} = 11.92\,nH \tag{4.20}$$

This approximation results in a stray inductance of $L_{DC} = 11.92\,nH$, which is slightly less than the average 12.4 nH that was predicted by software. This is of course only an approximation of the stray inductance's value, but it verifies that the stray inductance is in the ballpark of design range, which is within safe margins as the converter operates with a nominal current of $200\,A_{RMS}$.

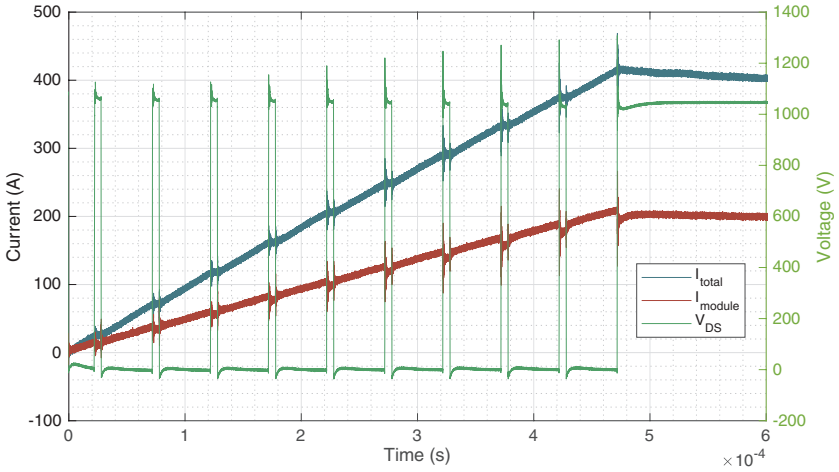


Figure 4.27: V_{DS}, and currents of a single leg during the fence tests. Overvoltage measured at the last turn-off event.

Summary

As it can be observed from the presented results, the converter was successfully putted into operation while complying with the corresponding design requirements and grid-codes for the tested operation point conditions. From the results it can be summarized that:

- The converter is capable of controlling its DC-Link voltage and output currents while connected to the grid.
- The measured NTC temperatures suggest that the loss model results are adequate to estimate the device temperatures.
- The DC-Link presents low parasitic inductance, and although the bandwidth of the current does not allow for an accurate calculation of the stray inductance, the observed overvoltage responds to an estimated DC-Link stray inductance of 11.92 nH.
- The current sharing between modules is almost 1:1 for practical purposes, even after 45 minutes of continuous operation, validating the feasibility of module parallel connection under this method.
- The LCL-Filter is capable of complying with the EN61000-2-2 and the EC/TS 62578 norms at this operation point, being considered successful for differential mode filtering.

However, there are certain limitations corresponding the design, such as:

- An EMC-Filter was necessary to connect the converter to the grid without issues. This common mode issue was not in the scope of this study, being nonetheless an important future research topic.

- The critical design point was actually regenerative behavior at nominal current. However, this was not possible to evaluate in the present conditions due to the existing grid conditions. It is also irrelevant from a temperature perspective, as the heatsink is overdimensionated for this design.

4.6 Summary

In the present chapter the design requirements, design criteria and final implementation of the converter has been presented. From this procedure, the main achievements are the following:

- Regarding loss estimations: an analytic method for loss calculation including third quadrant behavior was calculated to determine conduction losses, and along with known results of switching loss estimations in converter operation the losses of the converter were calculated. These results were in turn used to validate simulation results, which were based in PLECS with the experimental data of the characterization experiments in order to verify its correct operation.
- Regarding simulation of load profiles: a simulation method that considered the thermal model provided by the industry partner was developed. This method decouples the simulation of the two stages by simulating the fast time constants in one simulation (module time constants) and the slow time constants (heatsink time constants) by considering that only accuracy at $T_J = 125°C$ was necessary to achieve a good approximation. These results were then in turn validated through a fully modulated simulation to verify their validity and correct approximation errors.
- Regarding the determination of the nominal current: the presented simulations that determined the nominal current to be driven in the SiC converter demonstrator used in a first instance data originated from the single module experiments, and then its results were updated based on the module parallel connection data. The final conclusion of both simulations was that the nominal current of the converter was to be $200\,A_{RMS}$, hence the converter would be able to operate at 240 kVA.
- Regarding DC-Link design: the guidelines and procedure to design a low inductive DC-Link were presented. Here the capacitor selection, DC-Link bus bar design and simulation of parasitic inductance was presented. Results show that a low inductive design is achievable while complying with capacitance requirements in traditional rack designs.
- Regarding filter design: An LCL-Filter able to comply with the agreed upon grid-codes has been presented. This is part of the dissertation of Marcus Mueller and hence only the main requirements, considerations and resulting design has been presented. Here two important conclusions in the scope of the questions of this dissertation were determined. In a first approach, the i^2t of SiC diodes can be a limiting factor in filter design, especially when compared with Si-IGBTs, as the smaller die area of SiC devices seems to limit them in this regard. However, SiC Schottky diodes also have the MOSFET body diode in parallel, which should start conduction after in an inrush current event if the MOSFET is turned off. Hence a direct answer is not possible at the moment and this topic remains open for further

research. The second aspect is that filter design in this switching operation range at these power levels is a topic for which off-the-shelf solutions are very limited/non existent, and hence the craftsmanship and expertise of particular manufacturers plays a significant role in the possible filter solutions achievable for the particular emissions requirements generated by the SiC converter.

- Regarding the final results: The presented converter demonstrator has designed, implemented and tested at a 400 V_{ll} grid. The final validation test consisted on operation at nominal current with reactive power. Under these test conditions, the converter operated successfully, while also complying with the required grid-codes for differential mode, sharing current among modules in close to 1:1 ratio and presenting low magnitude overvoltages while driving nominal current. Regarding common mode, an additional EMC-Filter has been required to be able to operate the converter and be within norms. However, this was not part of this investigation and remains as future research topic.

5 Comparison and Assessment of the SiC-based Converter

In this chapter, the reader will find a theoretical comparison between two converter designs, which is performed in order to be able to fairly assess the advantages and limitations of silicon carbide in industrial applications for 690 V grids when compared with a silicon-based design. The comparison is performed following the design guidelines laid out in chapter 4, and considers loss, efficiency, weight and cost in order to perform the analysis. The selected power modules are the same that were used to compare Si-IGBT and SiC-MOSFET modules in the characterization section. It should be noted, that parts of this section were published in [95], which is available to the reader in open access format.

5.1 Comparison of a SiC-based and a Si-based Power Converter Design

As it was explained in chapter 4, the converter demonstrator uses a cooling system that is overdimensioned for the designed converter of 240 kVA. However, the experimental invetigation proofed both the converter design procedure and converter design. To enable a fair and useful comparison of converter designs with SiC-MOSFETs and Si-IGBTs, a second converter design has been done using both silicon and silicon carbide modules in order to perform a comparison of their characteristics regarding loss, efficiency weight and cost. This comparison is theoretical, but it is based on the experimental characterization of both modules presented in chapter 3 and published in [16] (see Fig. 3.30 and Table 3.11 for details) to estimate the converter losses, maximum nominal current and temperature rise in semiconductors. This in turn is used to calculate the passive component values required to comply with the design, to then propose a converter implementation based on off-the-shelf market components. This way, even without the actual converter construction of both designs, the resulting cost, size and weight of both converters will correspond with market available parts, thus providing reliable data of how the converter mechanical and electrical characteristics would be. Furthermore, the predicted data regarding loss, as proven by the temperature prediction models, is a good approximation based on the characterization of both devices, hence should produce reasonable results when used as input to the design process.

Important disclosure: the presented LCL-Filter was also designed by Marcus Mueller, and hence its results corresponding the design and filter considerations are of his own authorship. His main considerations are to be summarized here, but for a full description of the design process the reader is invited to read [95].

Table 5.1: Main converter requirements and design objectives.

Converter Requirements	
Topology	3Ph-2L-VSI
Grid voltage V_{ll}	690 V
DC-Link	V_{DC} = 1080 V, low inductive
Harmonic Standards	VDE-AR-N 4100 + EN61000-2-2(+A1/A2) IEC/TS 62578
Desired Max. Avg. T_J	125°C
Ambient temp. T_{amb}	45°C
Control	VOC with SVM
Comparison requirements	Identical nominal power and reasonable switching frequency for both designs

5.2 Methodology and requirements

To perform this comparison, or any comparison for that matter, the conditions and constraints of the comparison are crucial to frame the results for two important reasons. First of all, because these conditions and constraints will limit the design choices and hence are necessary to weight the results, as these are not universal but constrained to the conditions. And second of all, they are also important because the "Conditions of a comparison make the result of the comparison", as the limits imposed by the comparison could favor one design over another.

In this case, the presented comparison aims to contrast the characteristics of a SiC based converter design and a silicon-based converter design for the same output power, while presenting a reasonable switch utilization and switching frequency for their corresponding designs. The reason for these constraints is that both converters should be a solution for a given industrial application that requires a determined nominal power while at the same time their parts should be reasonably utilized to their potential.

The selected converter configuration for the comparison is also the three-phase two-level inverter, and it was to be implemented with a single module per leg, while at the same time be connected to a 690 V grid. Inheriting some parameters from the implemented design, the corresponding DC-Link was to be film based, and perform with a DC-Link voltage of 1080 V. Grid standards to comply with are the VDE-AR-N 4100, EN61000-2-2 and IEC/TS 62578, being among the main differences that now an LCL-Filter with a passive damping resistor was to be implemented as filtering solution. The ambient temperature and maximum desired device junction temperatures have also been kept as presented in the original design for the same reasons, and T_J = 125°C is the maximum recommended operating temperature for both modules. A summary of the corresponding requirements and topology summary can be found in Table 5.1 and Fig. 5.1 respectively.

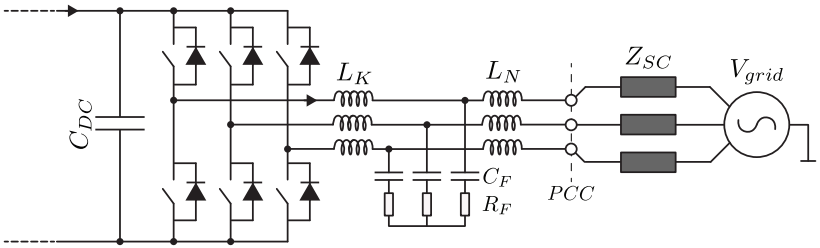


Figure 5.1: Diagram of the proposed topology for comparison purposes: the grid-tied 2L-VSI with LCL-Filter and passive damping.

5.3 Converter Designs

5.3.1 Determination of the Operation Point

By using the corresponding characterization information for both modules, simulations have been carried out for several frequencies and peak currents for the critical modulation index (M = $\frac{2}{\sqrt{3}}$) and Cos(φ) = [1 -1]. In every operation point, the case temperature has been iterated until it was possible to achieve all junction temperatures inside the corresponding modules below 125°C. Then, with this case temperature, and total loss of the three modules, a required thermal impedance from case to ambient could be determined. The conditions of the simulations are presented Table 5.2.

Table 5.2: Simulation parameters for the determination of the operation point

Simulation Parameters	SiC-MOSFET design	Si-IGBT Design
Switching Frequency f_{sw}	16 to 24 kHz	1 to 5 kHz
Peak current per module $\hat{I_N}$	150 to 250 A at 10 A steps	
Ambient temperature T_{amb}	45°C	
Cos(φ)	[1 -1]	
$R_{G(on)}$	0.8 Ω	3.3 Ω
$R_{G(off)}$	0.6 Ω	4.7 Ω

Based on these parameters, the resulting case temperatures can be used to determine the required case to ambient thermal resistance by using:

$$R_{th_{CA}} = \frac{T_{case} - T_{amb}}{3P} \tag{5.1}$$

where P is the loss of an individual module. Hence the total required case to ambient thermal impedance is calculated, and their corresponding curves can be found in Fig. 5.2.

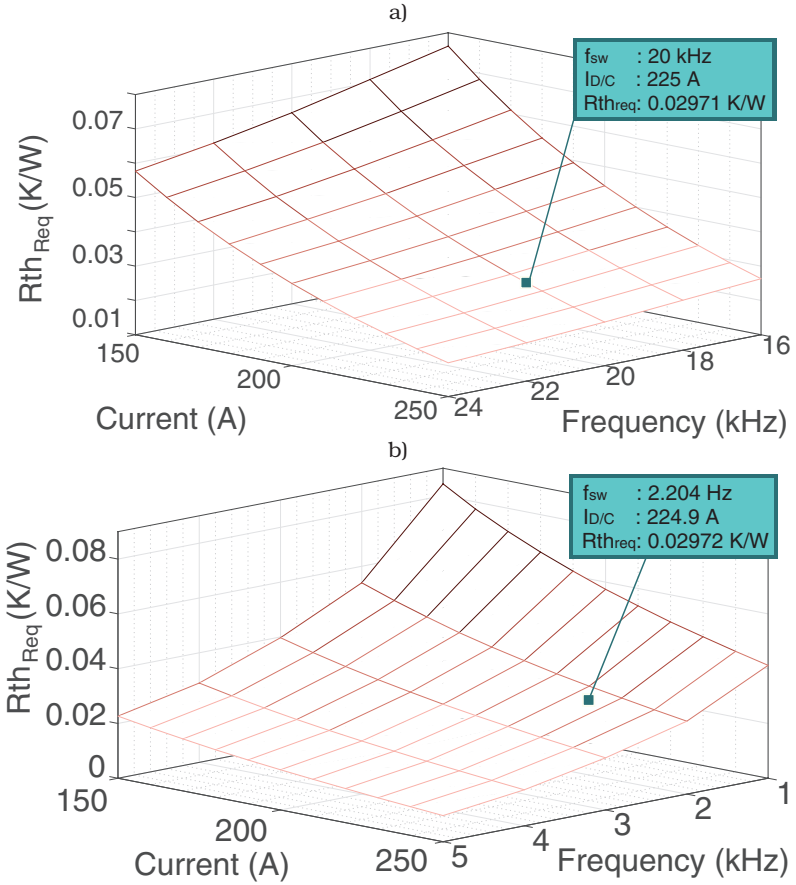


Figure 5.2: First approximation to the necessary R_{th} required for three modules over a heatsink. a) SiC-MOSFET based design, iterated from 16 to 24 kHz. b) Si-IGBT based design, iterated from 1 to 5 kHz.

Table 5.3: Comparison driven design objectives.

Comparison Driven Design Requirements		
Switching frequency f_{sw}	SiC-MOS: 20 kHz	Si-IGBT: 2.25 kHz
Nominal current I_N	159 A	
Nominal power S	190.14 kVA	
Required Rth_{c-a}	0.02867 K/W	

From the obtained curves in Fig. 5.2, it was determined that there were points that could present a good trade-off of driven current and switching frequency for both designs. In the case of the SiC-based design, switching frequencies over hearing range are achievable while not being too high to require expensive magnetic materials. And among these frequencies, a reasonable driven current yield could be achieved. On the other hand, in the case of the silicon-based design, it was possible to obtain an equally current capable design that was able of performing with a similar amount of loss, while still switching over the 2 kHz mark, hence being in the supra harmonic range where grid-codes are less strict. This enables a reasonable filter design, while also switching at a frequency standard industrial converters in some circumstances feature. During this process it was observed that also the same case to ambient thermal impedance requirement was available for both designs, which means that both converters could use the same cooling solution, simplifying a degree of freedom in the comparison criteria while at the same time not compromising output power or the comparison in a significant way. Furthermore, the available thermal resistances required for both designs were in the realm of what is physically possible [96] and what market available solutions could provide. After the operation point candidates were selected, additional simulations with more precision (the presented points in the datatips in Fig. 5.2 are interpolated points on the surface) were performed, and it was determined that both designs could achieve the same thermal impedance requirement and switch at a reasonable frequency with one single compromise: the SiC device at this critical operation point runs in average temperatures 2.46°C colder than the Si-based design (see Fig. 5.7). However, the advantages of the selected point, such as reasonable output current in contrast with their nominal capability, while enabling reasonable switching frequency points for both designs with a single realizable cooling solution was deemed as reasonable trade-off for an otherwise excellent operation point for a fair comparison between both designs. The final operation point is presented in Table 5.3.

5.3.2 Gate Unit

The used gate unit concept to characterize the devices was presented in Fig. 3.13. However, improvements over the used gate unit for the characterization of single devices (GUV1) were performed with the two following versions and are considered necessary for a new implementation. Thus, they are also summarized here and in Table 5.4. The gate unit must comply with the basic requirements presented in subsection 3.2.4, but some advanced characteristics are required as well. As presented in the gate unit section, is of particular importance for the SiC device that inductive paths in the driving loop are minimized. This means,

Table 5.4: Gate unit requirements.

Parameter	SiC-MOSFET design	Si-IGBT design
Turn-on Voltage	18 V	15 V
Turn-off Voltage	-2 V	-15 V
Peak current	10 A	3.9 A
Gatedriver power per switch	680 mW	167 mW
Shortcircuit protection	Desat detection	
Additional	Soft Turn-off, low inductive paths, symmetric construction, error detection	
High qty. cost	≈ 120 USD	

the driver needs to be as close to the driving pins as possible and overlapping driving/return current paths are desired [97]. DC/DC converters with small parasitic capacitances are also required to reduce common mode currents crossing the isolation barrier. Short circuit detection is also desired, and can be implemented for both technologies through DESAT detection method [80] with soft turn-off, with the consideration that in SiC the complete detection/protection process should not last more than 3 µs [98]. Additional considerations such as crosstalk attenuation and active clamping can be considered, but since no related effects during the characterization process were observed no countermeasures have been included in this particular design. Cost estimations were based on the desired components for the construction of the gate unit, such as DC/DC converter costs for 1700 V devices, optocouplers, ceramic capacitors and PCB.

5.3.3 Cooling Solution Design

The main criteria for thermal design is the required case to ambient thermal resistance defined as in (5.1), in which P is the loss of one module. Please note that both designs share the same nominal power and required $R_{th_{C-A}}$, but do not share the same case temperature or device loss as it can be observed in Fig. 5.6. Once the operation point of both converters was defined, it was only required to fulfill the prescribed R_{th} with an effective cooling solution comprised by the sum of thermal compound and heatsink thermal impedances. The complete selected thermal solution can be found in Table 5.5.

For the selection of the thermal compound, the Wacker P12 [99] has been chosen as its characteristics are suitable for module applications. It has been used in several setups at the TU-Dresden chair of power electronics (so its characteristics are known), and it is the thermal compound of choice of Semikron modules, company that specializes in device packaging and module construction [100, 101]. From the presented sources, it was also determined that an 60µm layer was a reasonable thickness for these modules. Additionally, it was considered that due to chip positioning inside the module not all the baseplate area would be used for heat transfer, hence a 90% of the total baseplate area was considered for the thermal resistance calculation. Since the heat transfer between module and thermal paste is purely conductive, the calculation of the thermal resistance between case and the heatsink right below the modules is straightforward, and calculated as

Table 5.5: Thermal design summary.

Heatsink Parameters	
Model	Fischer elektronik LA HL 3 200
R_{th} (v = 6 m/s)	0.025 W/K
Boxed volume	387 x 115 x 200 mm^3
Weight	10.75 kg
Fan Characteristics	
Model	Ebmpapst 4656N
Power (per device)	19.5 W
Weight (per device)	0.55 kg
Thermal Compound	
Model	Wacker P12
Thickness δ	60 μm
Module baseplate area A	62 mm x 122 mm
Relative effective baseplate area ε	90%
Thermal conductivity λ	0.8 $\frac{W}{mK}$
Total thermal resistance	0.00367 K/W
Summary	
Total Thermal resistance	0.02867 K/W
Total Weight	12.4 kg
Total Loss	58.5 W
High qty. cost	410 USD

$$R_{th_{TP}} = \frac{\delta}{3\varepsilon A\lambda} \tag{5.2}$$

were the corresponding variable symbols are to be found in Table 5.5.

Finally, regarding the heatsink thermal resistance, due convection heat transfer mechanisms a simple calculation of the thermal resistance based on material thickness and area is typically not possible, being finite element analysis techniques normally required to simulate their corresponding behavior. Thus, a high heatsink surface area usage is recommended [84] in order to get the thermal resistance values the manufacturer advertises, as typically the whole heatsink surface is either heated up or simulated for heatsink R_{th} characterization. Several heatsinks were considered, but the Fischer elektronik LA HL 3 200 [20] was selected because of its outstanding low thermal resistance values, and also because its thermal impedance was determined with smaller devices compared to the modules (80x43 mm^2 according to the manufacturer), and hence the nominal datasheet parameters can be considered as a worst case scenario. A diagram of the corresponding heatsink and the manufacturer temperature curves can be found in Fig.5.3.

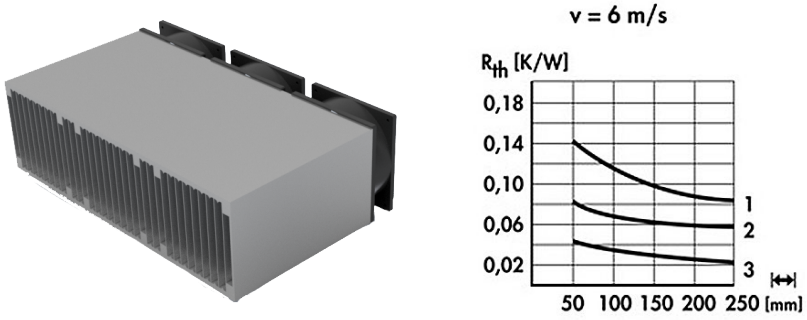


Figure 5.3: Heatsink: Fischer elektronik LA HL 3 200 mm (R_{th} 0.025 K/W) [20]. Left: 3D model of the heatsink. Right: Thermal impedance curves for one, two and three aggregates with heat sources on top.

5.3.4 DC-Link Design

As mentioned in section 4.3, the DC-Link has the task of acting as energy buffer and providing a stable voltage for modulation purposes. The corresponding design criteria for the design of this DC-Link follows the same guidelines of the presented design in chapter four, hence film capacitors have been used and the same design criteria for capacitance selection and bus bar design has been employed with the sole difference that in this case, there were no space limitations as there is no physical rack to comply with.

Regarding capacitor parameters, in this case the main criteria for designing the DC-Link capacitance for both converters was the power to energy ratio as seen in (4.18), opting for a relative conservative design. Regarding current limits, the worst case scenario through the DC-bank was calculated based on the work in [89] (just as in the corresponding section), resulting in 79.55 A.

It is important to remark, that film capacitors have been selected for both converter designs. This decision is a practical one for comparison purposes, as different DC-Links for both designs would be possible but would extend the comparison without providing substantial additional insight. Due to its form factor, capacitance and weight the FFLI6U0267KJE from AVX was selected for this study, which suit perfectly to reach the desired capacitance, while also fulfilling RMS current requirements.

Finally, the DC-Link bus was designed with 2 mm thick copper bars isolated through a 0.25 mm Hostaphan RN foil. The DC-Link concept also features a small distance between the capacitor bank to the module connections, to homogenize the observed stray inductance from all module connections and distance itself from the heat sources. This space is however small, to not substantially increase stray inductance. Simulations with Altair Flux 2018 have been performed over the design, and the obtained stray inductance (considering capacitor's ESL) is 15 ± 0.5 nH from every module connection. A summary of the DC-Link design and corresponding diagrams can be found in Table 5.6 and Fig. 4.14 respectively.

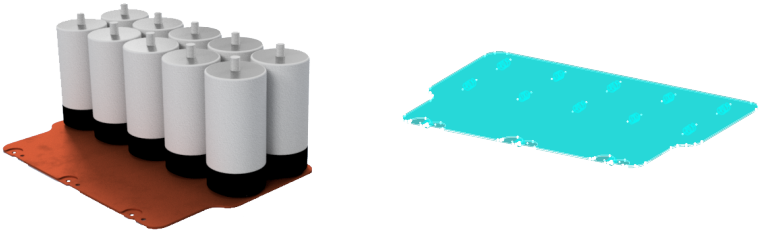


Figure 5.4: left: Designed 3D model of the DC-Link bank. Right: 3D Parasitic inductance analysis through Altair Flux 2018.

5.3.5 LCL-Filter Design

As seen in the previous chapter, the main function of the filter is to keep the harmonic emission in compliance with several grid-codes. In this particular case, to accomplish a fair comparison three different standards were considered:

- VDE-AR-N 4100 [102] This norm limits harmonic voltage emissions and currents are given up to 9 kHz, with the remark that if the harmonic current limits are not met, it's only necessary to met the harmonic voltage limits.
- IEC/TS 62578 [103] Contains only compatibility levels for external voltage distortion, which can be used for filter design with 3 dB safety margin.
- EN61000-2-2 [104] Recommendations for harmonic voltage emissions up to 150 kHz are proposed.

Hence, and as previously explained, only differential voltage distortion limits at the PCC were considered. Additional considerations in the design were:

- The grid impedance was not considered to be purely inductive, as mentioned in the LCL-Filter section in chapter 4.
- This filter considered a passive damping solution, as there are standard passive damping solution in the market as off-the-shelf devices for silicon devices already. Both converters designs will feature this filtering solution.
- Based on market off-the-shelf solution grid side and converter side inductor proportions, and choosing a low damping ratio that presents a good trade-off between loss and harmonic emissions, while complying with grid-code requirements and presenting resonant frequencies between reasonable margins, there are still infinite combinations of inductance and capacitance values to design the devices. Hence the total energy stored on the filter was minimized to reach the final filter realization.

Considering these factors, the final filter parameters were obtained and can be found in Table 5.7. Regarding their physical realization, the manufacturer Schmidbauer presented a design for the inductive filter components. On the other hand, TDK EPCOS capacitors for AC filtering have been selected as fil-

Table 5.6: DC-Link design summary.

DC-Link Requirements	
DC-Link Capacitance	2.6 mF
Max RMS current	79.55 A_{RMS}
DC-Voltage	1080 V
Additional	Low inductive
Selected Capacitor	
Manufacturer	AVX
Model	FFLI6U0267KJE
Capacitance	260 µF
ESR	5.6 mΩ
ESL	50 nH
Max. I_{RMS}	42 A
Quantity	10
Weight per unit	0.85 kg
High qty. cost	102.49 USD/unit
DC-Link Bus Bar Design	
Material	Electrical Quality Copper
Weight	2.61 Kg
Isolating material	Hostaphan RN
Isolating capability	19 kV @ 0.25 mm
DC-Link Design Summary	
DC-Link Capacitance	2.6 mF
Parasitic inductance	15 nH
Total DC-Link weight	11.1 kg
High qty. cost	≈ 1200 USD

ter capacitors. Particularly, capacitors from the the B32370 and B32374[1] families for the SiC and Si converters were selected respectively. Finally, chassis mounted resistors from Arcol line HS 150 have been chosen for damping, as they can dissipate 45 W without a heatsink. The design summary can be found in table: 5.8.

[1] Price was approximated to 50 USD/unit using other references in the same family

Table 5.7: Filter nominal parameters.

Module	L_K/µH	L_N/µH	$C_{F,y}$/µF	R_F/mΩ
Si	940 (6.8%)	470 (3.4%)	135 (18.1%)	327 (7.6%)
SiC	190 (1.3%)	95 (0.7%)	20 (2.6%)	270 (6.3%)

Table 5.8: Filter design summary, cost values in $ USD.

		L_K	L_N	$C_{F,y}$	R_F
Volume	Si	58.1 dm^3	30.1 dm^3	3.08 dm^3	0.61 dm^3
	SiC	21.9 dm^3	10.0 dm^3	0.52 dm^3	0.21 dm^3
Weight	Si	150 kg	65 kg	1.15 · 3 kg	0.175 · 9 kg
	SiC	50 kg	20 kg	0.21· 3 kg	0.175 · 3 kg
Cost	Si	$ 2328	$ 654	$ 150	$ 108
	SiC	$ 1094	$ 246	$ 59	$ 36
Losses	Si	940 W	280 W	Negl.	375 W
	SiC	400 W	130 W	Negl.	106 W

5.3.6 Final Physical Layout and Summary

Finally the theoretical converter implemetation, along its main components and the corresponding LCL-Filter realization are presented in Fig. 5.5. The modules have been distributed to be centered to each cooling aggregate, while every DC-Link module input has been balanced to observe close to the same stray inductance. Both the air exhaust and the DC-Link support structure are there for reference purposes only. No support structures, cables, or protections have been numerically considered for this study to assess overall weight, volume or cost. This is also an important constrain, percentage weight and cost gains are to be reduced as more elements common to both structures are included.

Due to the nature of the comparison, and to the fact that both DC-Link and cooling solution are shared among designs, the main differences in the design of both converters are due to module costs and filter design. The corresponding filter design implementations are virtually presented in Fig.5.5 and, as it can be observed in the figure, the SiC converter presents important filter size reductions when compared to the Si based converter design, presenting close to two thirds of weight and volume reductions when compared with the proposed filter solution for the Silicon-based counterpart.

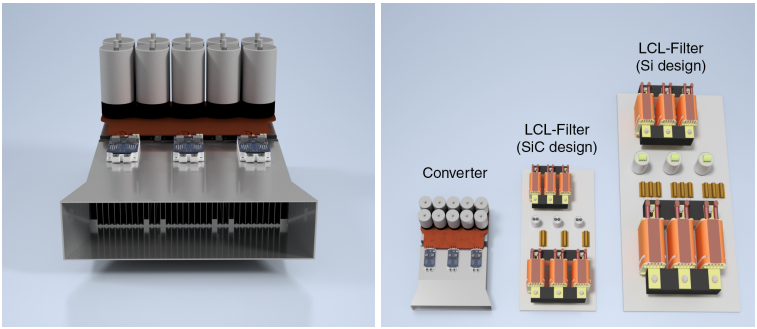


Figure 5.5: Physical Layout of the power converter. Left: 3D model of the 2L-VSI, including power block, cooling solution and DC-Link. Right: Graphical 3D comparison of the LCL-Filter solutions with the power converter as reference (only components are shown as reference, optimized LCL physical layout should vary).

5.4 Results and Evaluation

Finally, both designs are subjected to a comparison of their main characteristics regarding loss, efficiency, weight and cost. Starting by loss and efficiency, both rectification and inverter operation at unity power factor while using Modulation index M = 1.1547 (critical scenario) were performed and are presented in Figs. 5.6 and 5.8 respectively. As mentioned in section subsection 5.3.1, the critical design point presents itself in unity power factor by regenerative operation.

- Loss distribution and overall efficiency

  As seen in Fig. 5.6, both the IGBTs and the MOSFETs junction temperatures limit the nominal current of the converter presenting relatively similar semiconductor loss at the nominal point, hence being the filter losses the main source of loss differences at the nominal point. Regarding these filter losses, to estimate the losses in non-nominal operation points the inductor losses provided by manufacturer were assumed to be equally distributed between copper and core losses (as this is a valid optimization criteria for inductor design). By this assumption copper losses were extrapolated by estimating a winding resistance, and then losses to lower currents were calculated while leaving the core losses constant. In other words, at nominal currents the value is exactly as presented by manufacturer, being an extrapolation as soon as smaller currents are tested. As observed in the figure, both converter losses are outshined by filter loss for low currents, hence efficiency could be increased by using other filter strategies if they allow the usage of less core material or feature active damping schemes. When translating these losses into efficiency it can be observed that the SiC variant outperforms the silicon-based converter along the whole operation range, being also negatively affected by the filter for light loads, but presenting an overall behavior over 98% efficiency for almost the entire operation range.

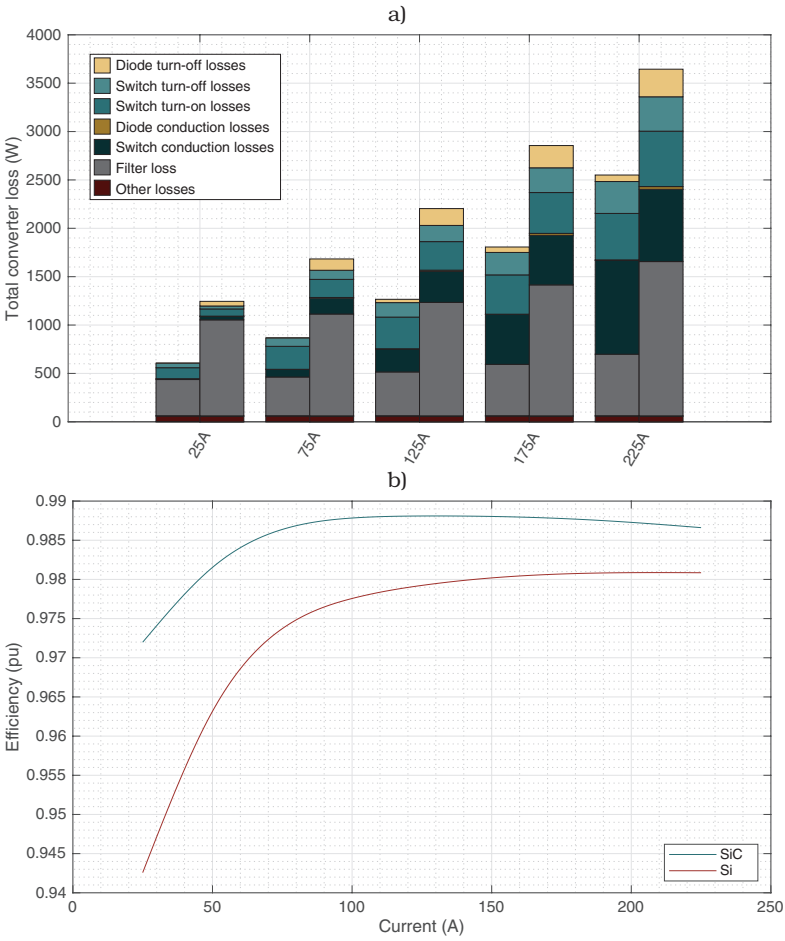


Figure 5.6: a) Converter loss distribution in inverter operation mode (PF = 1). SiC-MOSFET converter losses and Si-IGBT converter losses depicted in the left and right bar for every current respectively. Other losses comprise gate unit loss, heatsink fan loss, and DC-Link loss. b) Corresponding efficiency curves for the converter at PF = 1.

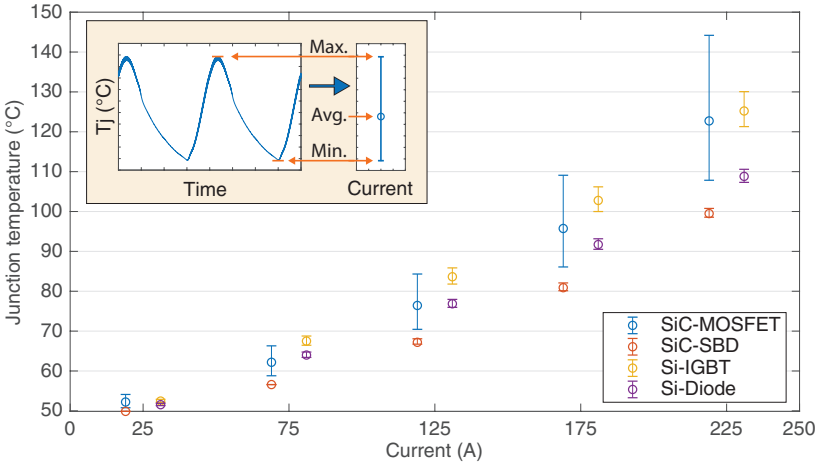


Figure 5.7: Converter junction temperatures in inverter operation mode (PF = 1). SiC-MOSFET module and Si-IGBT module junction temperatures depicted in the left and right bar for every current respectively. Note that the temperatures for both modules correspond for each point to the same current and have been only slightly shifted for better visibility.

Regarding junction temperatures, as it can be observed in Fig. 5.7 that although the design was made to make the SiC-MOSFET converter operate 2.46 °C colder in average than its Si-IGBT variant, the smaller die area of the SiC-MOSFET results in higher temperature oscillation in the switch when compared with the Si-IGBT variant, almost reaching 145°C. This is still within module specification, but this junction temperature oscillation of over 40°C peak-peak in nominal operation point could potentially generate power cycling issues. However, such reliability study goes beyond the scope of this work.

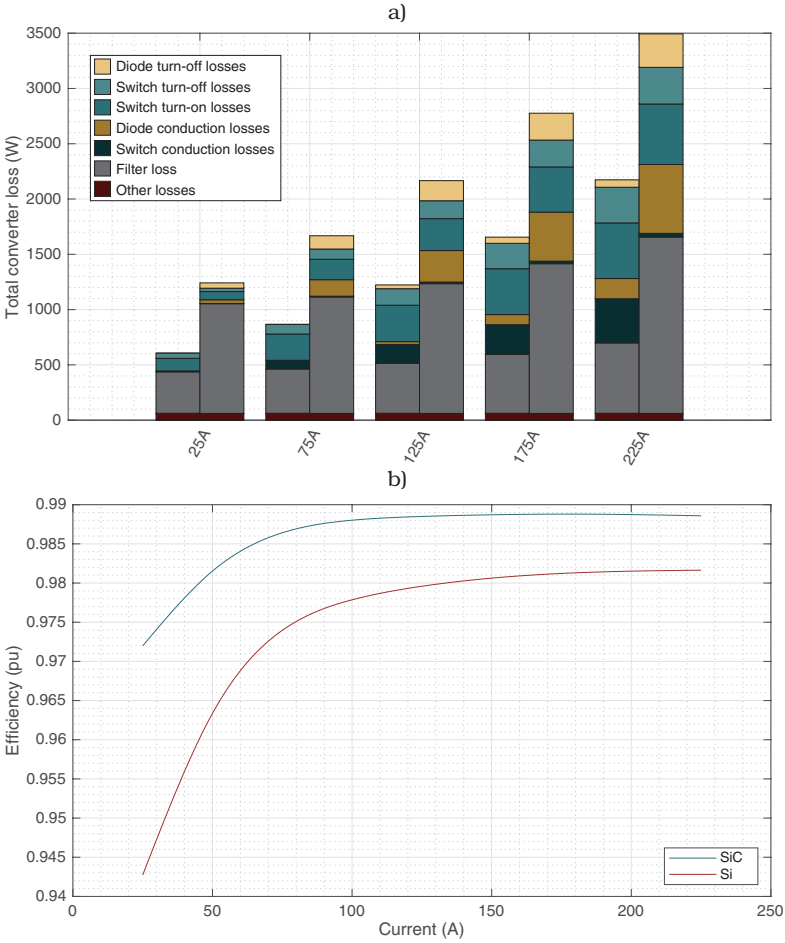


Figure 5.8: a) Converter loss distribution in rectification mode (PF = -1). SiC-MOSFET converter losses and Si-IGBT converter losses depicted in the left and right bar for every current respectively. Other losses comprise gatedriver loss, heatsink fan loss, and DC-Link loss. b) Corresponding efficiency curves for the converter at PF = -1.

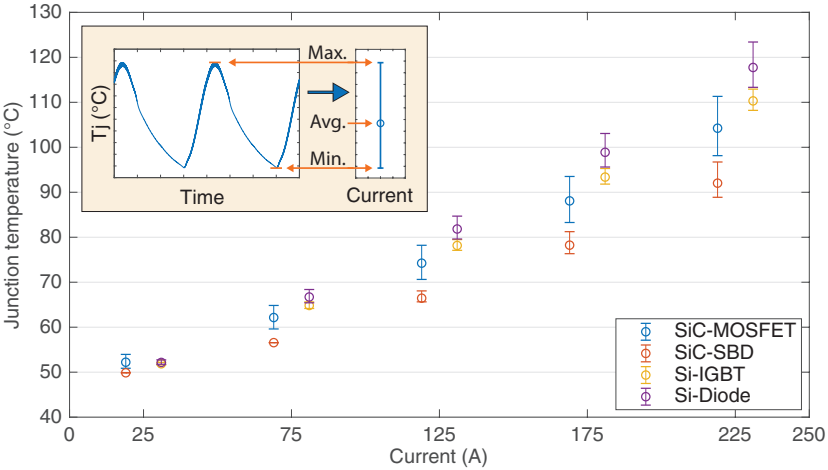


Figure 5.9: Converter junction temperatures in rectifier operation mode (PF = -1). SiC-MOSFET module and Si-IGBT module junction temperatures depicted in the left and right bar for every current respectively. Note that the temperatures for both modules correspond for each point to the same current and have been only slightly shifted for better visibility.

On the other hand, when observing rectification mode (see Fig. 5.8), it is possible to observe that the silicon based converter is outperformed by the SiC based variant. Due to the silicon diode loss characteristics of the IGBT module, and on the other hand, the current sharing between the MOSFET channel and its SBD (active rectification), the SiC variant presents even lower losses, which has a direct impact in the corresponding efficiency curves, presenting 98.9% at nominal operation point. Regarding the Si-IGBT module design, the bulkier filter, the diode reverse recovery and the forward voltage drop characteristic are the main factors of reduced efficiency at light loads, performing better the closer the device reaches nominal operation and reaching a 98.3% efficiency in this operation mode.

Regarding junction temperatures, as it can be observed in Fig. 5.9, both SiC devices in the module present lower junction temperatures when compared with the silicon-based design. This results are not only valid for average junction temperatures, but also peak junction temperatures with the sole exception of low load operation points, which are not critical. The SiC device observes MOSFET and diode average junction temperatures of $[T_{JM}, T_{JD}] = [104, 92]°C$ respectively, in contrast with the Si-IGBT module which presents $[T_{JI}, T_{JD}] = [110, 118]°C$ for IGBT and diode respectively at the nominal operation point. This showcases again the advantages of active rectification, as it is possible to observe how the loss sharing benefits SiC based converter junction temperatures.

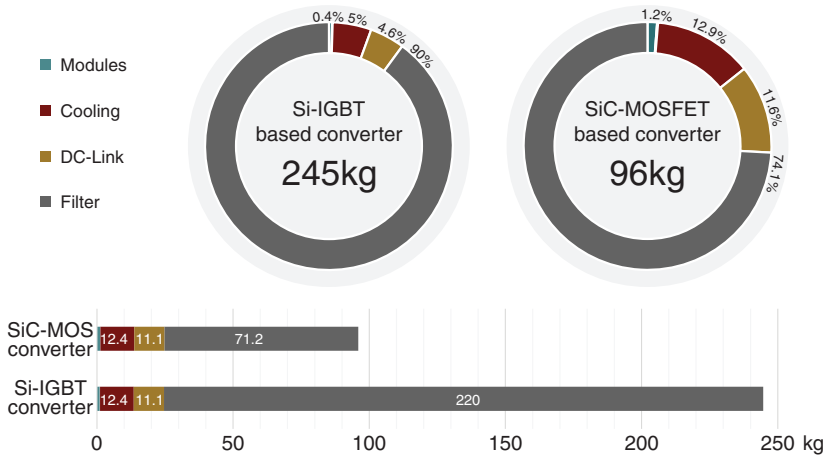


Figure 5.10: Comparison of percentage and total weight distribution of both converter designs.

- Weight and cost analysis

  When considering the weight comparison analysis (see Fig.5.10), even without considering the basis over which this comparison was made, it is a known fact that a significant part of the weight in a converter will be concentrated on the line inductors/line transformers because of the high density of their core materials (iron, silicon steel), added to their copper requirements. Hence, by rising the switching frequency almost tenfold, a significant reduction in the inductor weight is achievable (equivalent to a 67% reduction for the studied case), not only because of the switching frequency, but also because of the harmonic emission limit the filter must comply with, which obeys to a somewhat lighter constrain that what it would have been, if the same limiting norm for the 2.25 kHz filter requirement was just extrapolated. This heavily impacts the total weight of the converter, allowing the realization of a design based on silicon carbide that can pack 1.97 kVA/kg, vs the 0.77 kVA/kg the silicon-based converter variant could achieve under these conditions. Further weight reductions could be achieved when considering other core materials, but the increase in cost is hardly justifiable for this application.

  Finally, the cost distribution comparison of all converter components is presented in USD dollars in Fig. 5.11. Referring to cost distribution percentages alone, since the overall cost difference is not substantial, and both designs share several design choices, the differences basically originate in the trade-off between module costs and filter costs. Here, due to the sheer cost of the filter, the Si-IGBT based converter costs 10% more than the SiC based variant in spite of the lower semiconductor cost, showcasing the impact a larger filter has on the overall design. This result comes unexpected, as industrial grid connected infeeds have not been high in the lists of applications that

could benefit of SiC-module devices [105]. But, as it can be observed from the results, they have the potential to propose a cost effective solution while providing efficiency and power density improvements to these applications as well.

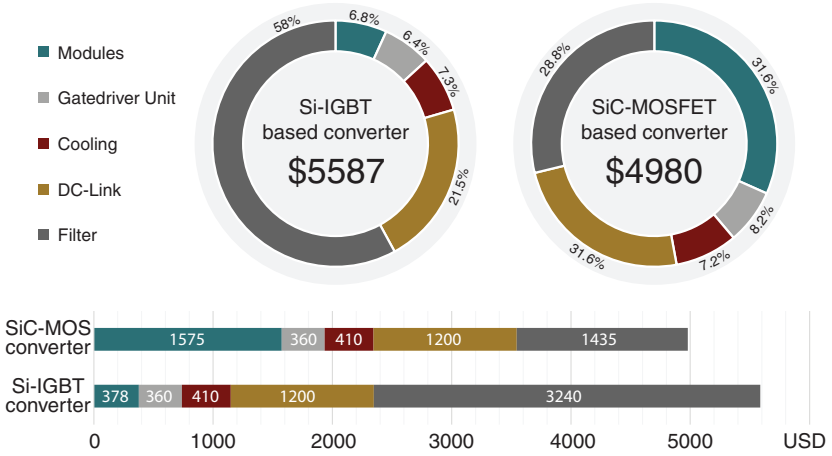


Figure 5.11: Comparison of percentage and total cost distribution of both converter designs.

Possible cost reductions for the Si-converter are nonetheless possible, such as slightly cheaper gate units due to reduced dv/dt immunity requirements and a wider selection of devices in the voltage driving ranges. DC-Link costs can also be reduced if electrolytic based capacitors are used instead. Additionally, light has been shed that the SiC converter can require an additional EMC-Filter to solve common mode issues, however this has not been studied as it was not in the scope of this study. Nonetheless, the fact in the cost distribution is clear: these changes (without considering the EMC-Filter) are not a big part of the costs of the converter and hence should not essentially change these results drastically, most likely leading to a gap reduction than a significant tip on the scales to the other direction. Furthermore, the inclusion of the corresponding support structures should be a bit more expensive on the silicon-based converter, as the support structures need to withstand a higher weight, and the extra weight and volume should also increase logistic costs.

5.5 Summary

In this chapter, a comparison between two grid-tied 190 kVA 2L-VSI SiC and Si converter designs for 690 V grids based on experimental characterizations and manufacturer's data has been performed. And to do so, a careful selection of the nominal operation point has been made to provide fair grounds to be performed. Results show that the SiC based design is able to provide superior efficiency in the whole operating range while remaining cooler in average. This at a 39% of the weight and with a 10.9% reduction in overall cost of important power component parts when compared with the silicon-based solution. Further optimization, other filter strategies, or filter realizations by different manufacturers and DC-Link cost reductions can be performed, which would possibly close the cost gap between both designs. Nonetheless the result remains: SiC devices can also be a profitable, interesting semiconductor material for industrial grid-connected converters, with the associated benefits of higher efficiency, power density, and switching frequency over hearing range, which would traduce in noise reduction in industrial environments, which all in of itself can already be a factor to tilt the scales towards a SiC based design.

6 Conclusion

Silicon carbide is an exciting wide bandgap semiconductor material filled with high potential due to the limitations in crystal manufacturing processes and packaging technology; which is why it is expected to keep innovating in the short to medium term. Solutions to the low channel mobility issues could further reduce the $R_{DS(on)}$ resistance, improvements in gate oxide reliability could open the path to trench devices in the 1700 V range and beyond, and improvements in packaging technology could and will allow these devices to operate with higher temperatures, a fact that will increase the maximum current output/switching frequency for the same die size, shaping new converter formats as this technology develops. In a relatively short timespan of five years (2015-2020) the SiC market exploded, quadruplicating its semiconductor offer and penetrating several markets at manufacture grade level, specifically in applications that highly rely on high efficiency or power density.

In this work, the realization of a grid connected three-phase two-lever industrial full-SiC converter demonstrator for 690 V grids has been investigated. To accomplish this, a thorough study of the off-the-shelf market selection of SiC devices has been performed, and with it, a SiC module has been selected and characterized in both single and parallel operation. In single module characterization experiments the device showed the capability of switching for up to 10 times less energy than a comparable Si-IGBT module variant, featuring switching rise/fall times in the 100 ns range and presenting small, but non-negligible reverse recovery loss. As the main drawbacks it presented a steep increase in dv/dt compared with Si-IGBT counterparts, fact that required careful considerations of common mode paths in order to prevent issues with its operation. On the other hand, when operated in parallel with another module, it presented good driving current symmetry in spite of high switching speeds while using this hard-connected kelvin source connection strategy. This behavior was further confirmed in converter operation, where the current distribution was almost 50/50. Additionally, it was proven that the third version of the gate unit presented safe current values through its kelvin source pins, ensuring safe long-term operation of the GU.

During the converter implementation stage of the work, it was demonstrated that the SiC device can operate with up to 10 times higher switching frequency than an equivalent Si-IGBT would require to operate at comparable power output. This had significant impact in the filter size, fact that can also be corroborated when observing the corresponding comparison. This increased switching frequency not only translates in filter size reductions, but also cost reductions as long as cost effective core materials are available for design. Furthermore, it can translate into possible efficiency gains. Additionally, a low inductive DC-Link design for the application was successfully developed, presenting very small overvoltages in spite of the fast switching speed of the SiC devices.

In summary, the final converter implementation demonstrated that the SiC converter could control power output with grid connection while complying with the required grid-codes successfully, but requiring an additional EMC-Filter to

operate correctly. This was not part of the study and it is reserved as an interesting future research topic. But, and notwithstanding the above, this converter demonstrator realization proved the point that, with careful consideration of common mode paths, symmetric construction, and low inductive layout designs, a SiC converter design can be performed successfully without significant caveats.

Additionally, and although the SiC demonstrator was overdimensioned due to its cooling solution, its construction aided to validate the design criteria and methodology to perform the theoretical designs that provided the grounds for a comparison between the SiC and silicon-based converters, concluding in the fact that the usage of SiC devices can decrease weight for industrial applications, while presenting efficiency improvements in the whole operating range at comparable cost. This result must however be considered as preliminary, as this result depends heavily on the possible realizations the inductor manufacturer is capable of providing, and non resolved issues such as the EMC-Filter and long term reliability concerns should also be addressed to then reevaluate the question. Further research is required to complete and extend the evaluation of SiC-MOSFET based industrial inverters. However, there are reasonable design criteria and considerations with real physical implementations today, that could make silicon carbide a cost-effective and technically interesting solution for this application under a determined set of reasonable constraints.

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